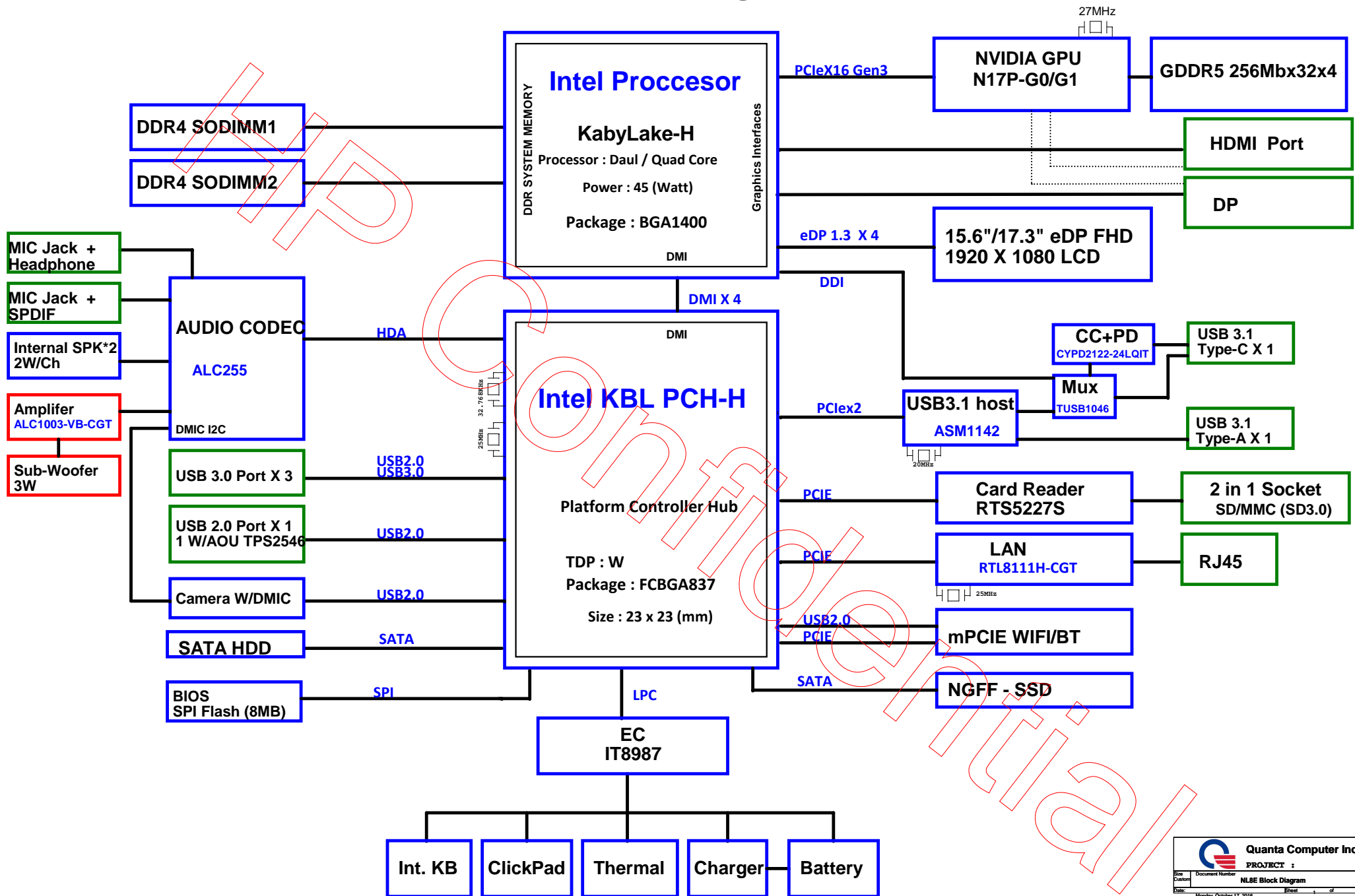


# NL8K Block Diagram

01

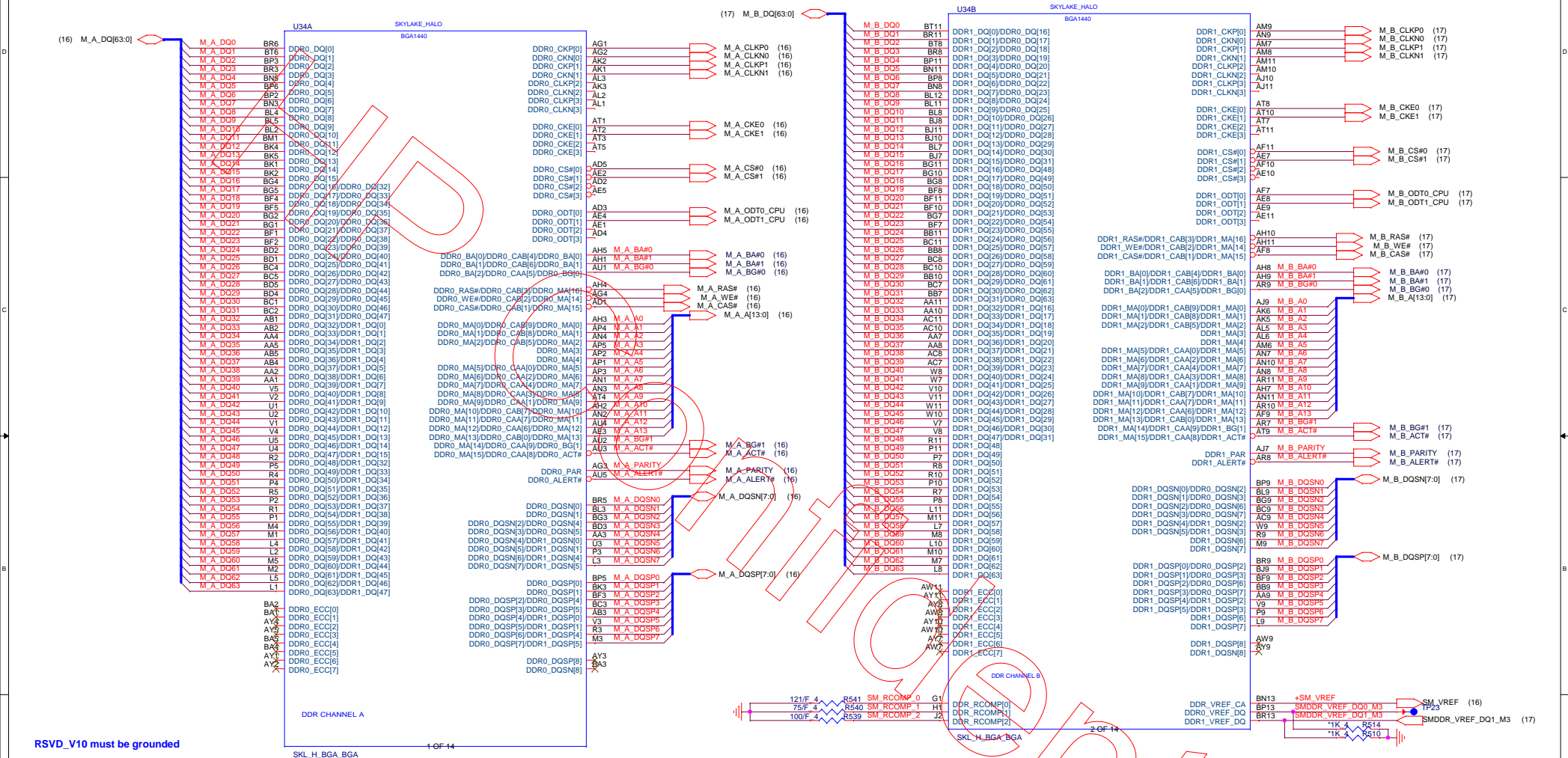


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+VCCIO (37,6)  
+1.2VSUS (10,16,17,2,35,43,44,50,6)  
+3V\_SS (10,12,14,21,23,25,26,27,28,31,32,34,37,38,39,43,49,52)  
+3V (10,11,12,13,14,16,17,18,19,20,21,22,23,24,26,27,28,29,30,31,32,36,43,45,50,52,9)

## SKYLAKE Processor (DDR4)



Follow SKL H EDS page 133 to 45W(GT4+OPC): +VCCGT=104A/12A (GTx)  
Follow SKL H EDS page 133 to 45W(GT2): +VCCGT=55A


4+4e, Support eDRAM Only, GTX 12A

+VCC\_CORE (40,44,7)  
+1.2VSUS (10,16,17,2,35,43,44,50,6)



VCCGT\_SENSE (39)  
VSSGTX\_SENSE (39)  
VSSGT\_SENSE (39)  
VCCGTX\_SENSE (39)

VCC Output Decoupling Recommendations		

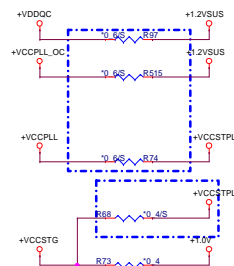


Quanta Computer Inc.

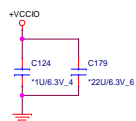
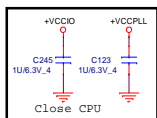
PROJECT :

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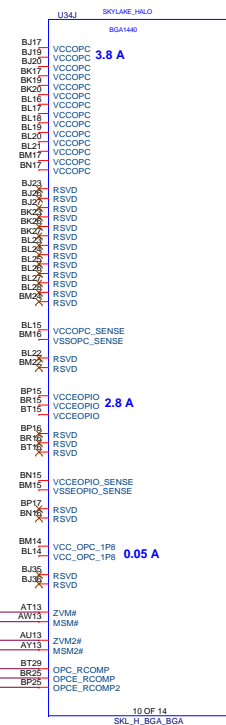
Follow SKL H EDS page 135 45W: VDDQ=2.8A

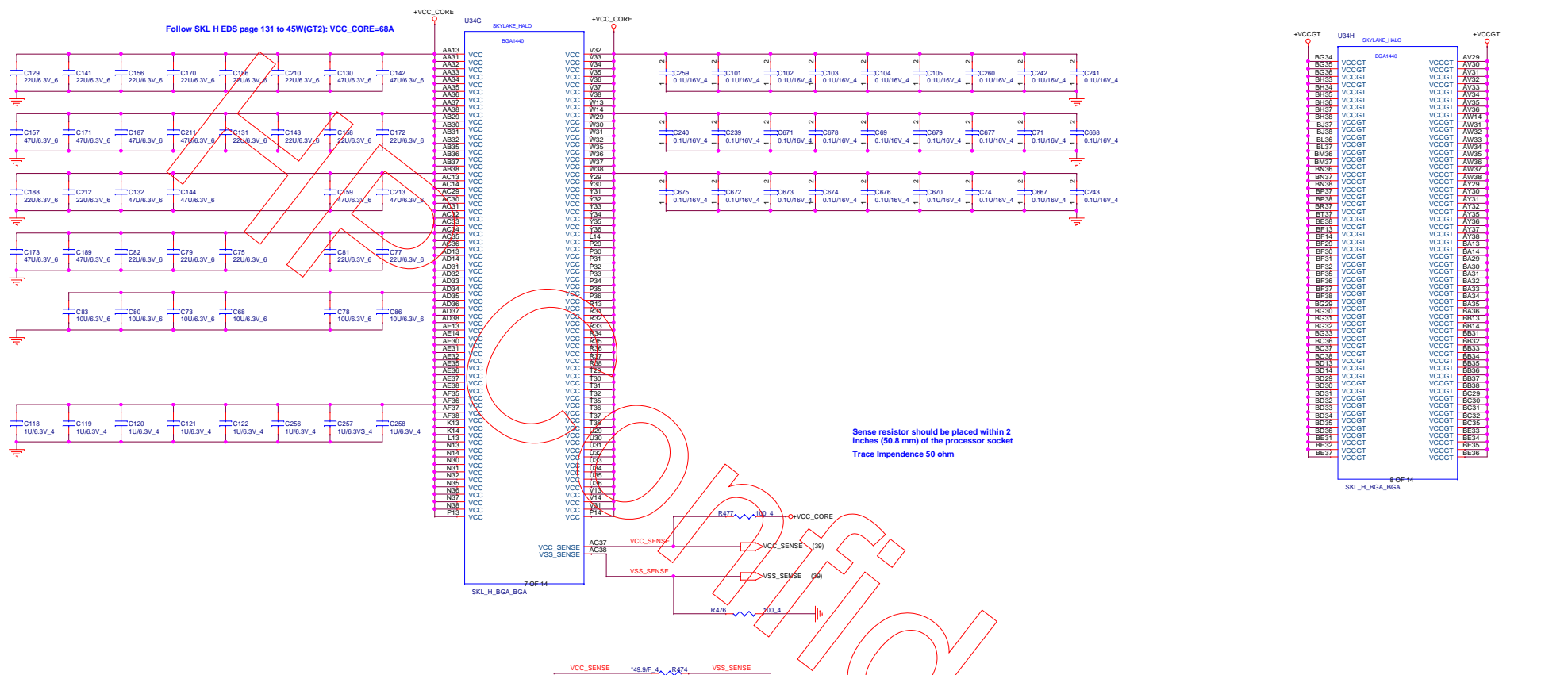


EDRAM Only, PLACE CAPS IN ACK SIDE



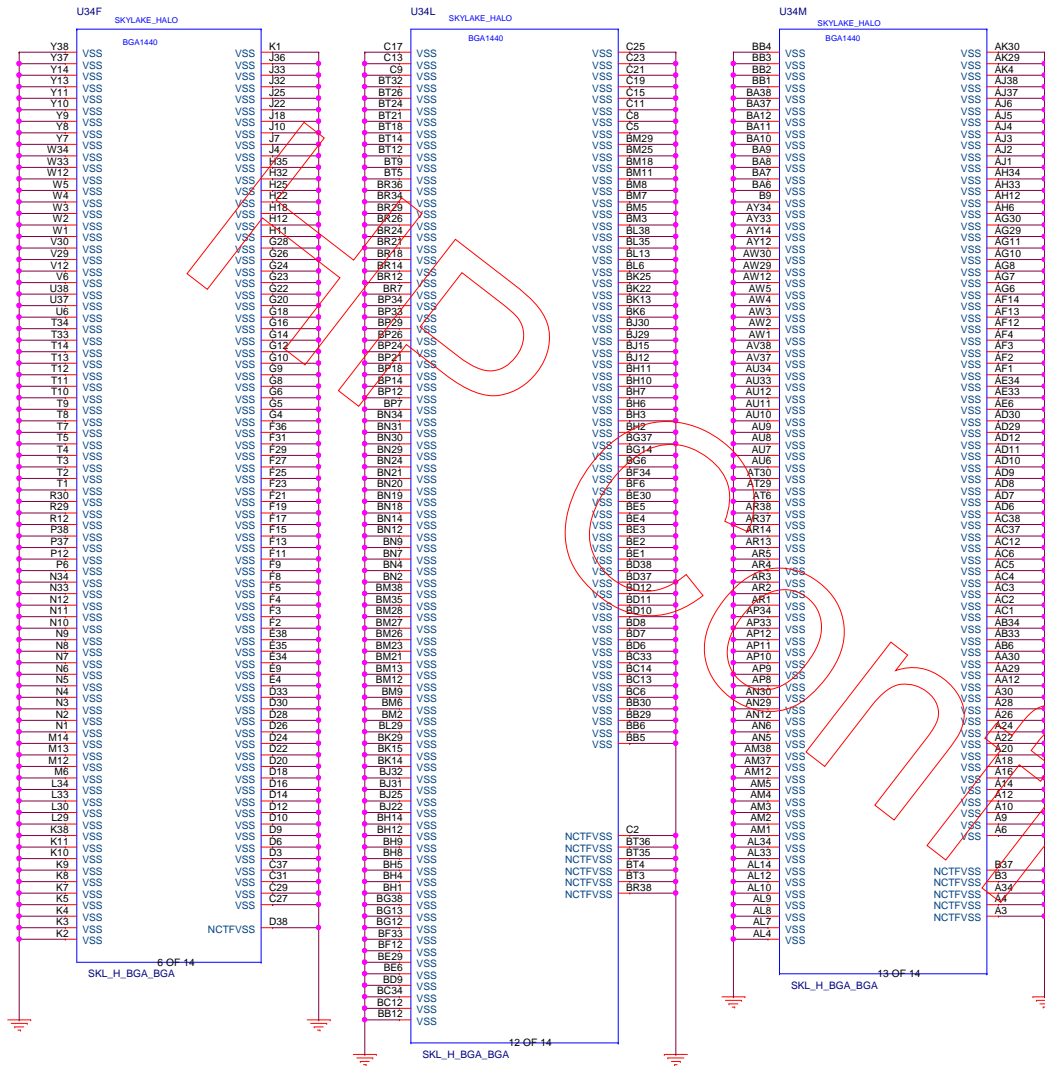
Unconnected for Processors without OPC.



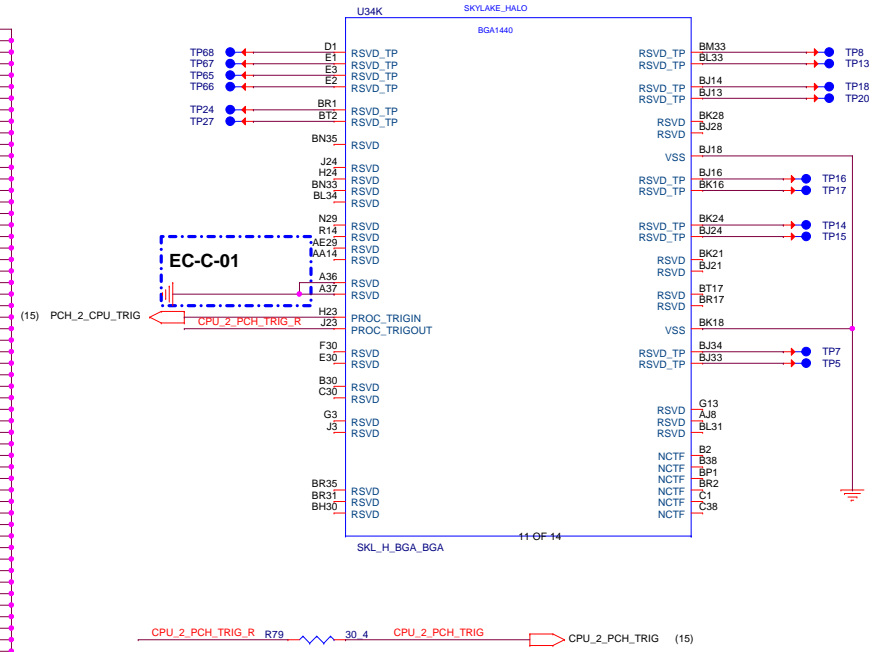




# Haswell Processor (GND)

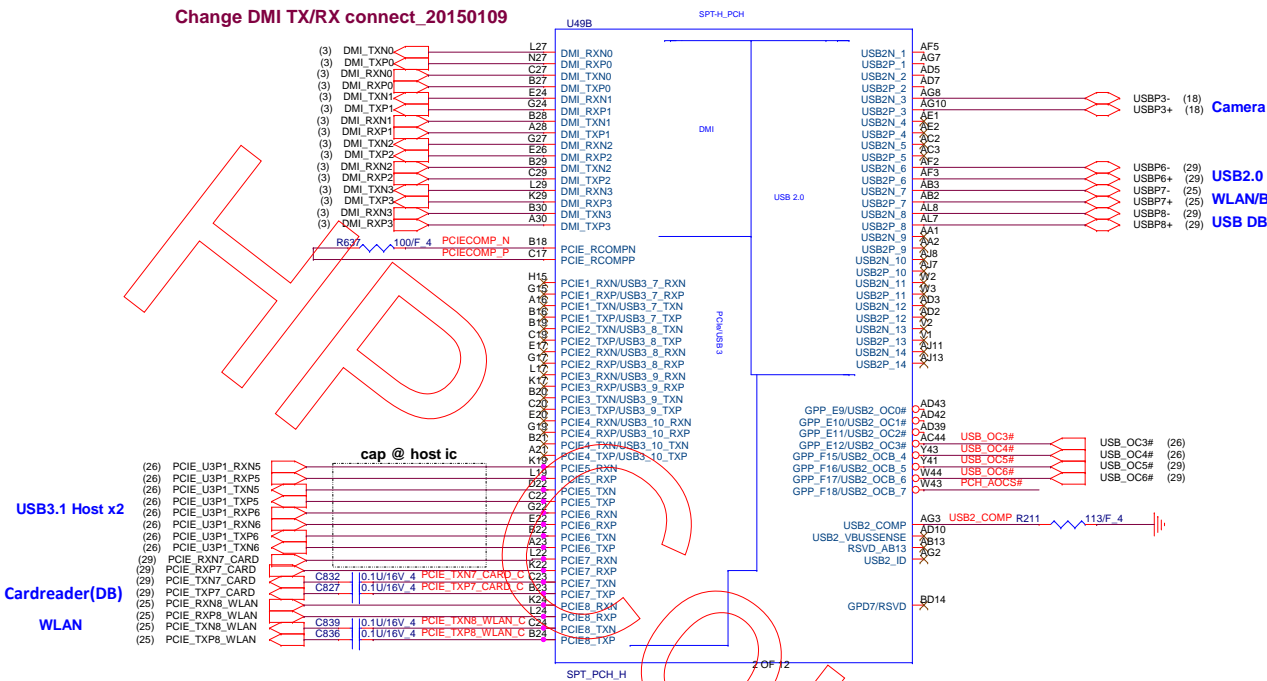


# Haswell Processor (RESERVED, CFG)





## Change DMI TX/RX connect\_20150109



## GPU Strap

**DFX TEST MODE**  
XTAL INPUT IS SINGLE ENDED IF  
SAMPLED LOW ELSE  
DIFFERENTIAL



### RING OSCILLATOR BYPASS



## XTAL INPUT FREQUENCY[0]



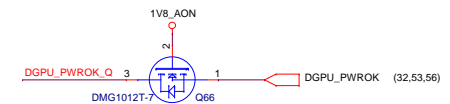
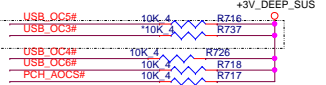
## XTAL INPUT FREQUENCY[1]



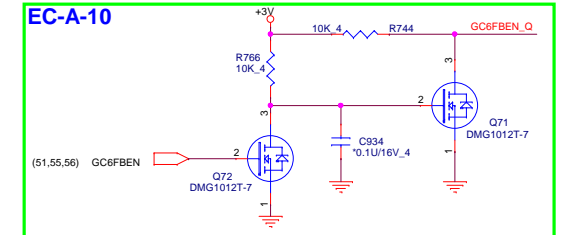
DGPU\_EVENT#-- For BIOS check



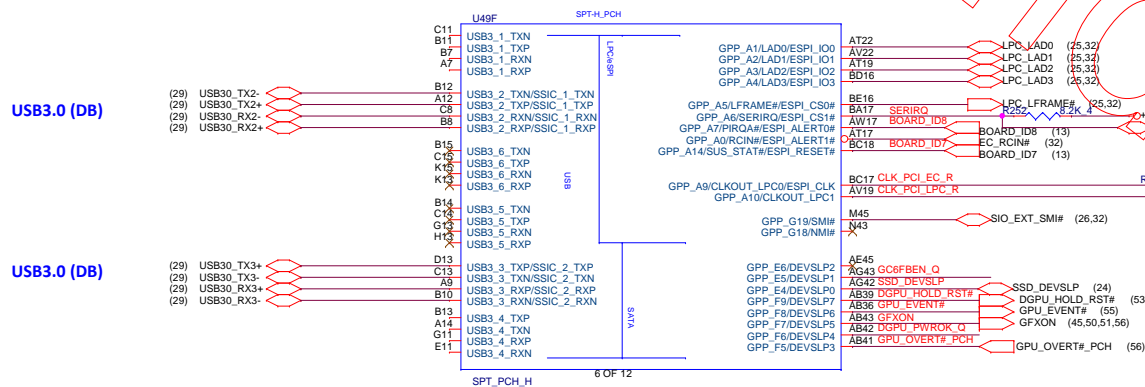
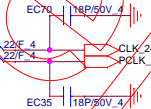
PU at USB3.1 host

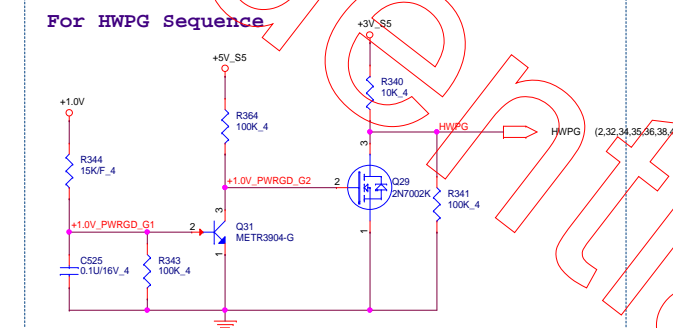
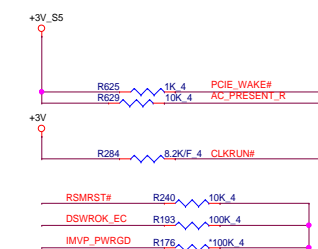
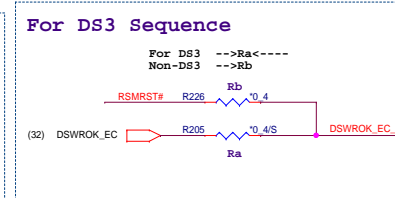
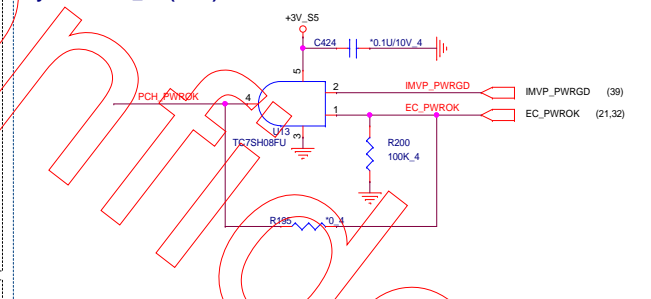


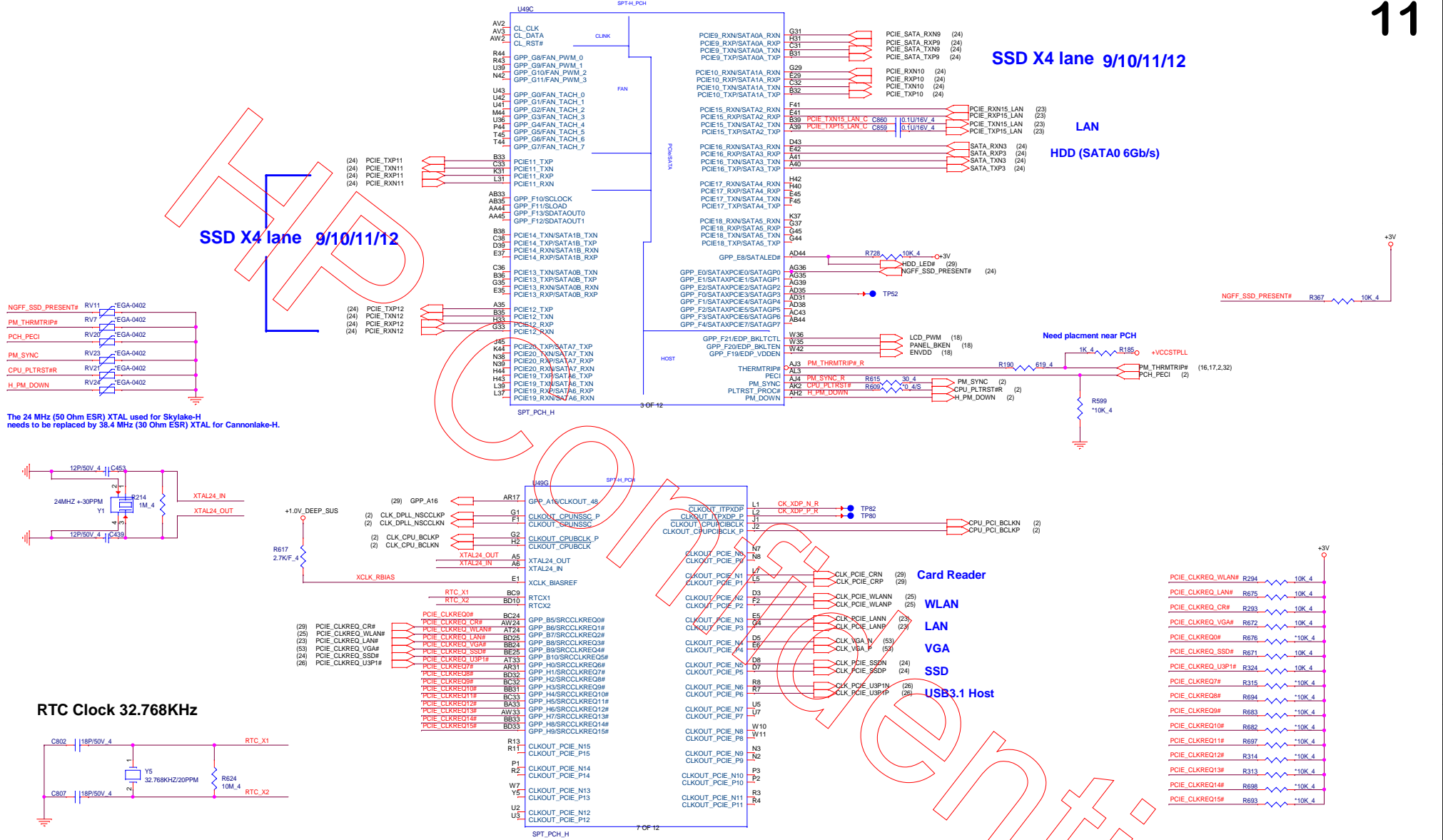
EC-A-10



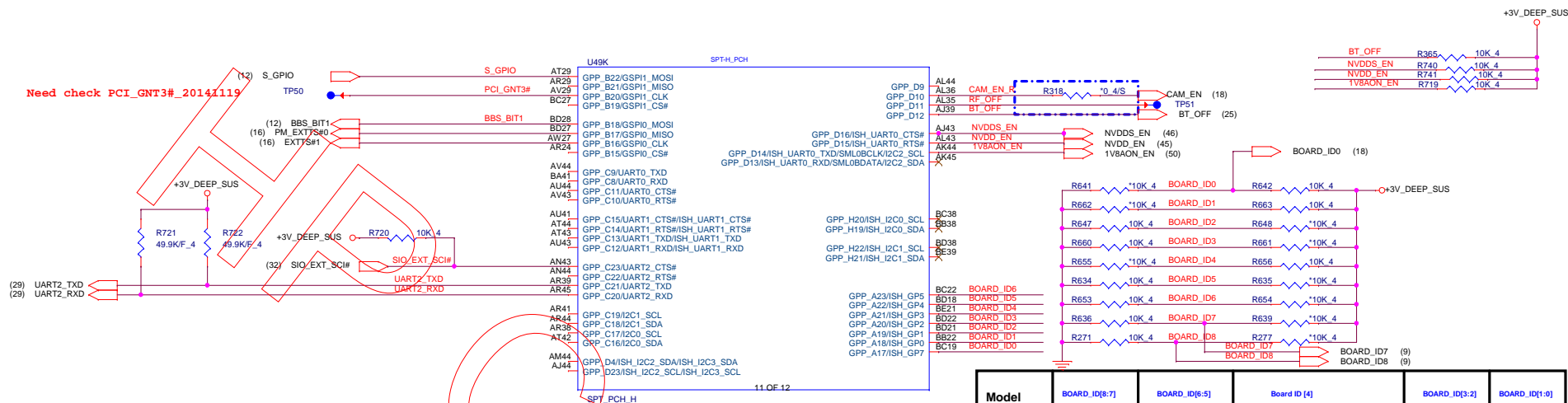
## EMI(near PCH)



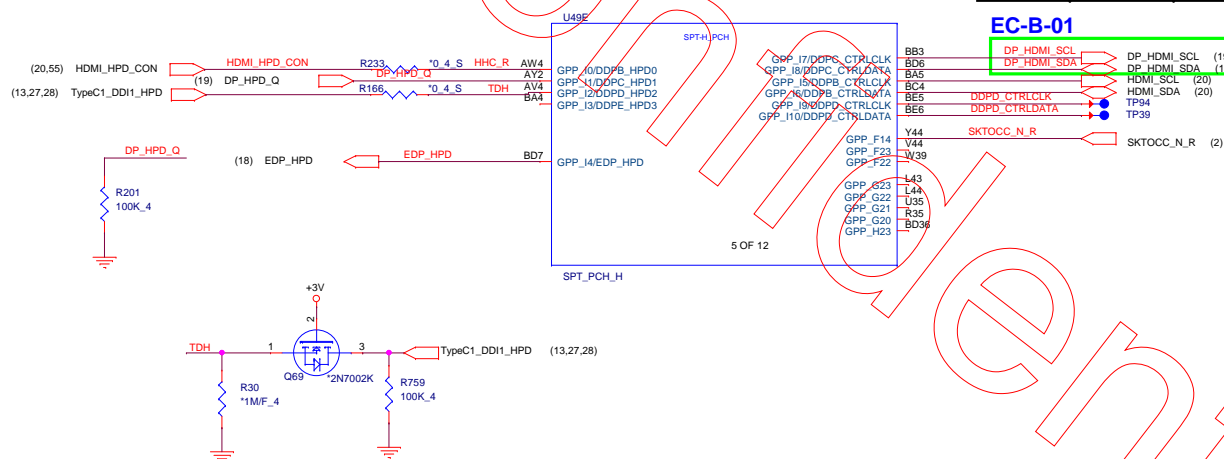
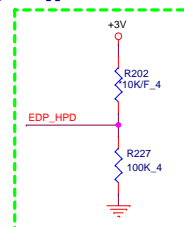




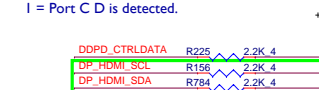


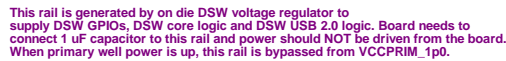


Reserve EDP\_HP\_D opposites circuit!

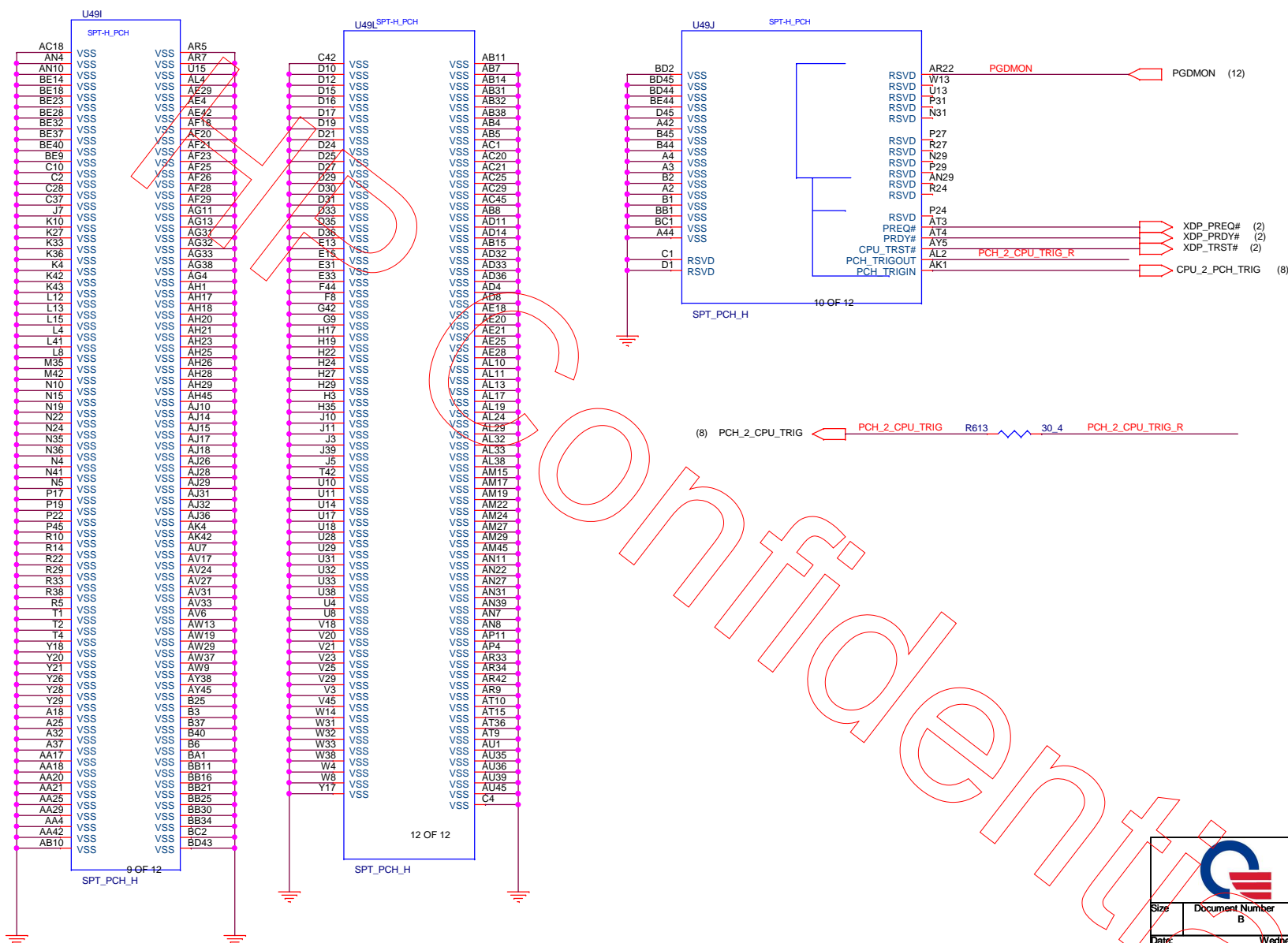


This signal has a weak internal pull-down.  
0 = Port C D is not detected.  
1 = Port C D is detected.

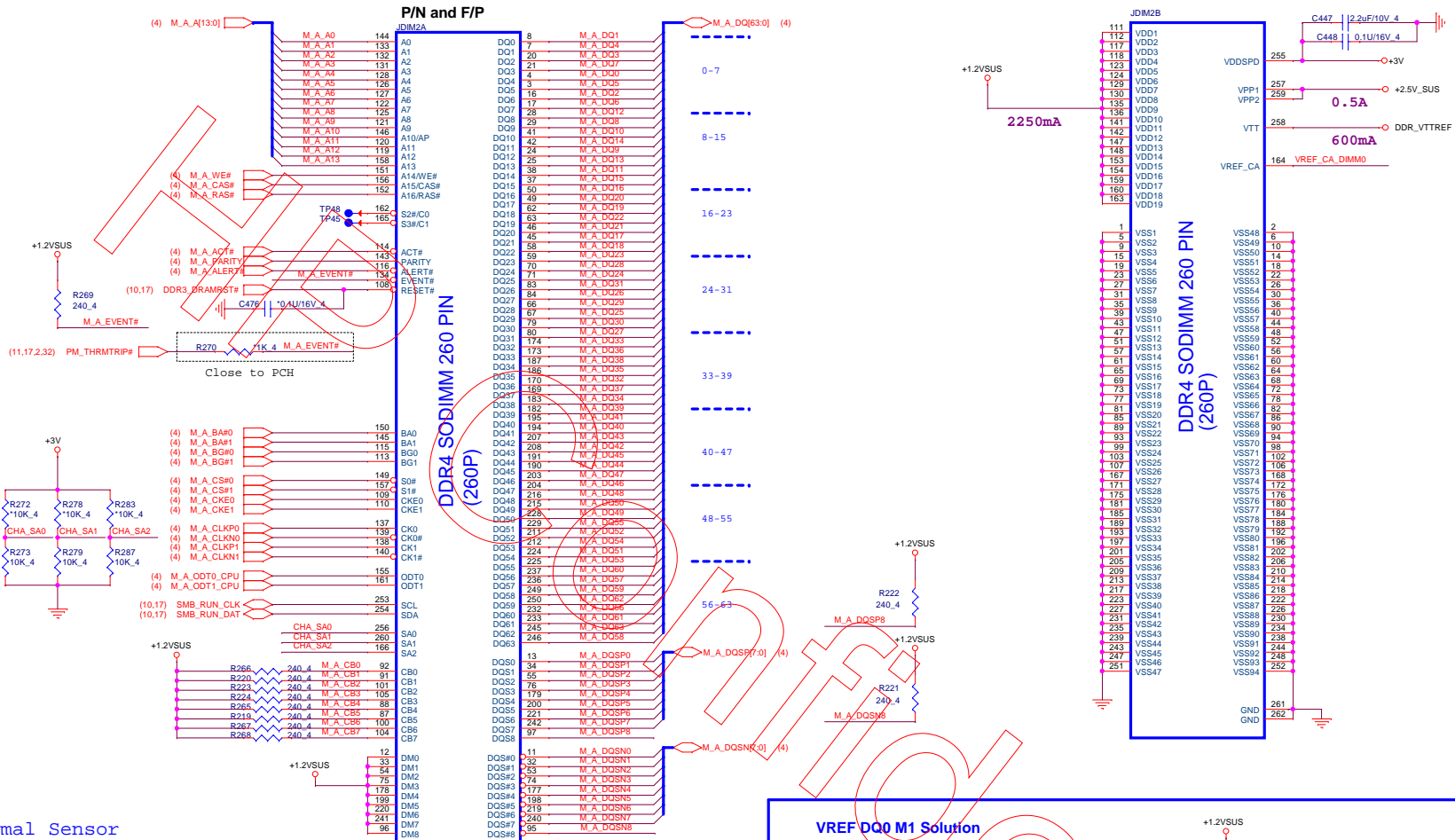


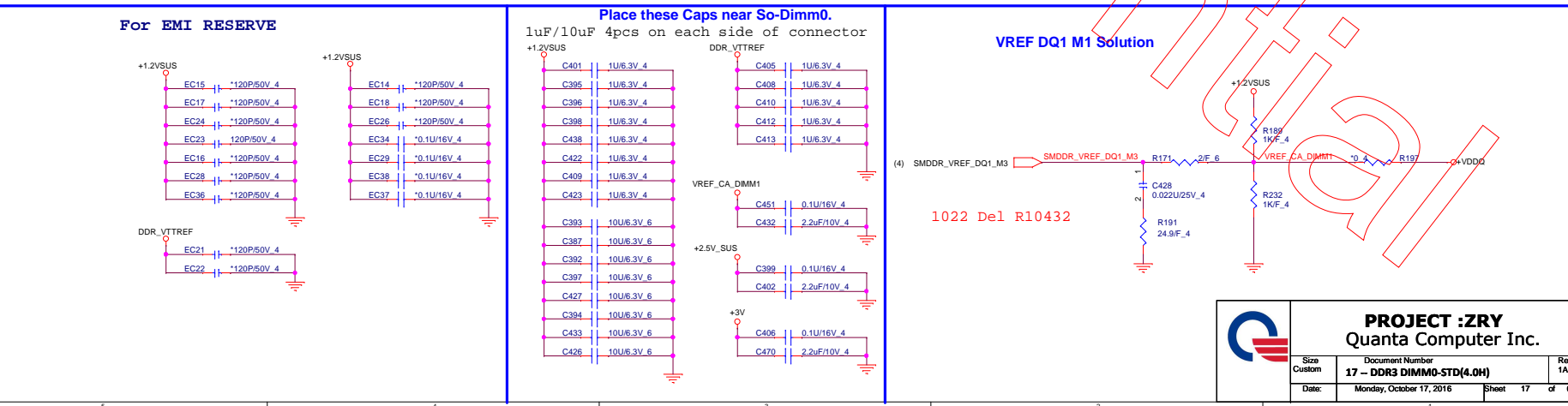




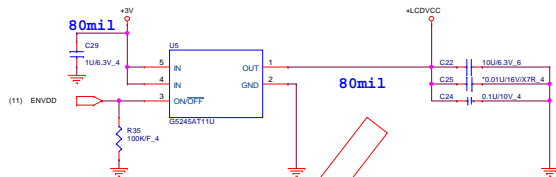




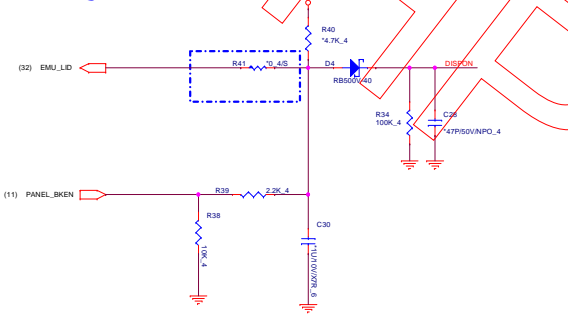




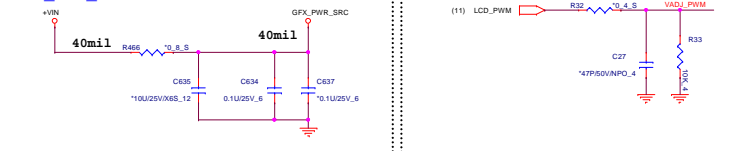
### LCDVCC



### Back light

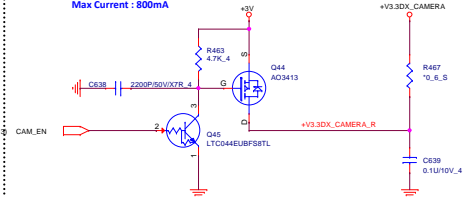


### GFX\_PWR\_SRC

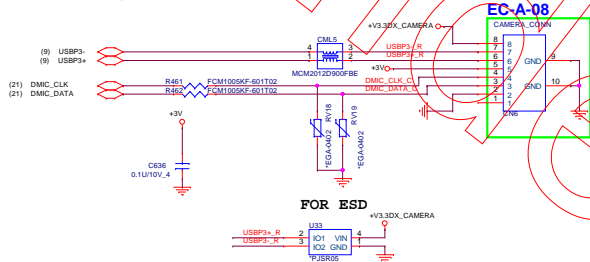


### CAMERA VCC Control

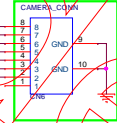
+CAM\_VCC  
Max Current : 800mA



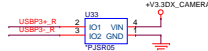
### CAMERA/DMIC CONN



### EC-A-08

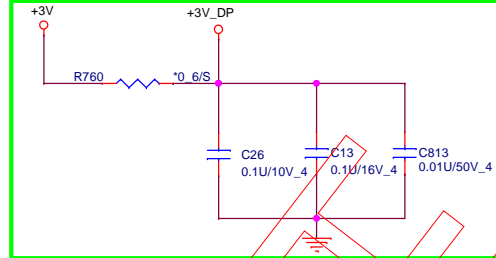


### FOR ESD

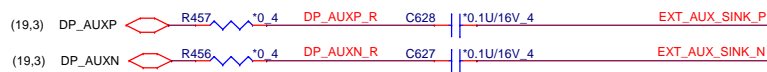
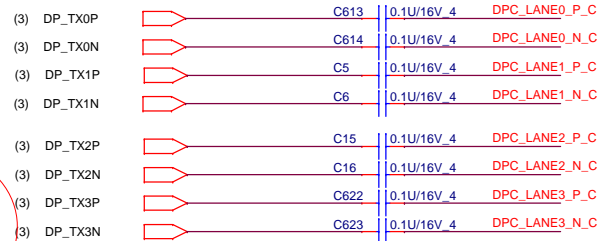
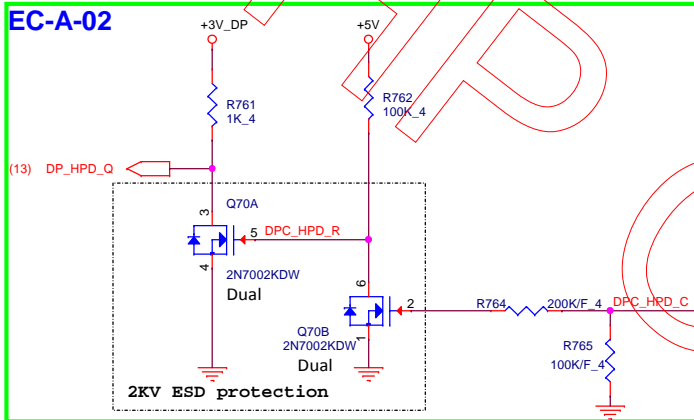


## EC-A-01

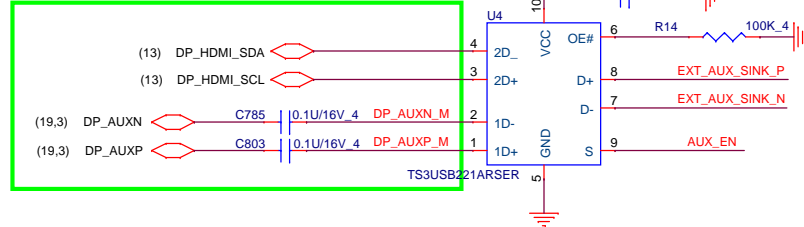
## EC-B-02



## EC-A-02



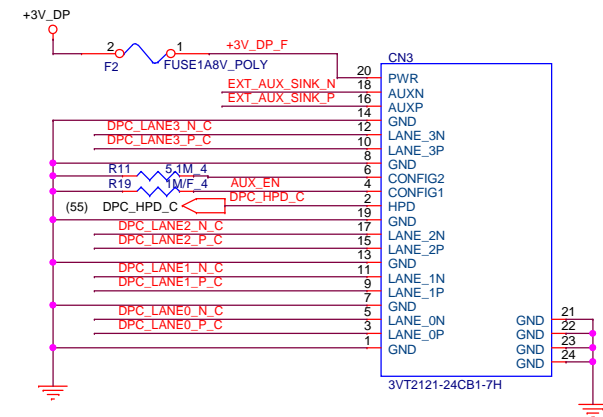
## EC-B-01



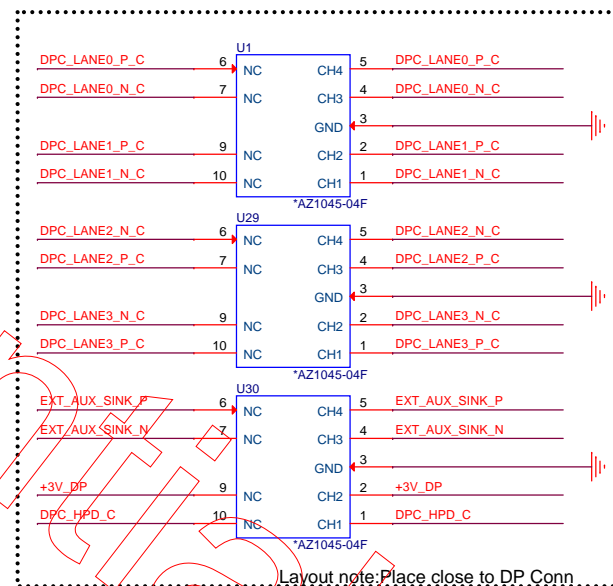
(10,11,12,13,14,16,17,18,20,21,22,23,24,26,27,28,29,30,31,32,36,43,45,50,52,9) +3V  
(20,21,22,24,30,31,43,45,52,63) +5V

+3V  
+5V

19



For ESD



Layout note: Place close to DP Conn

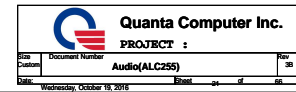


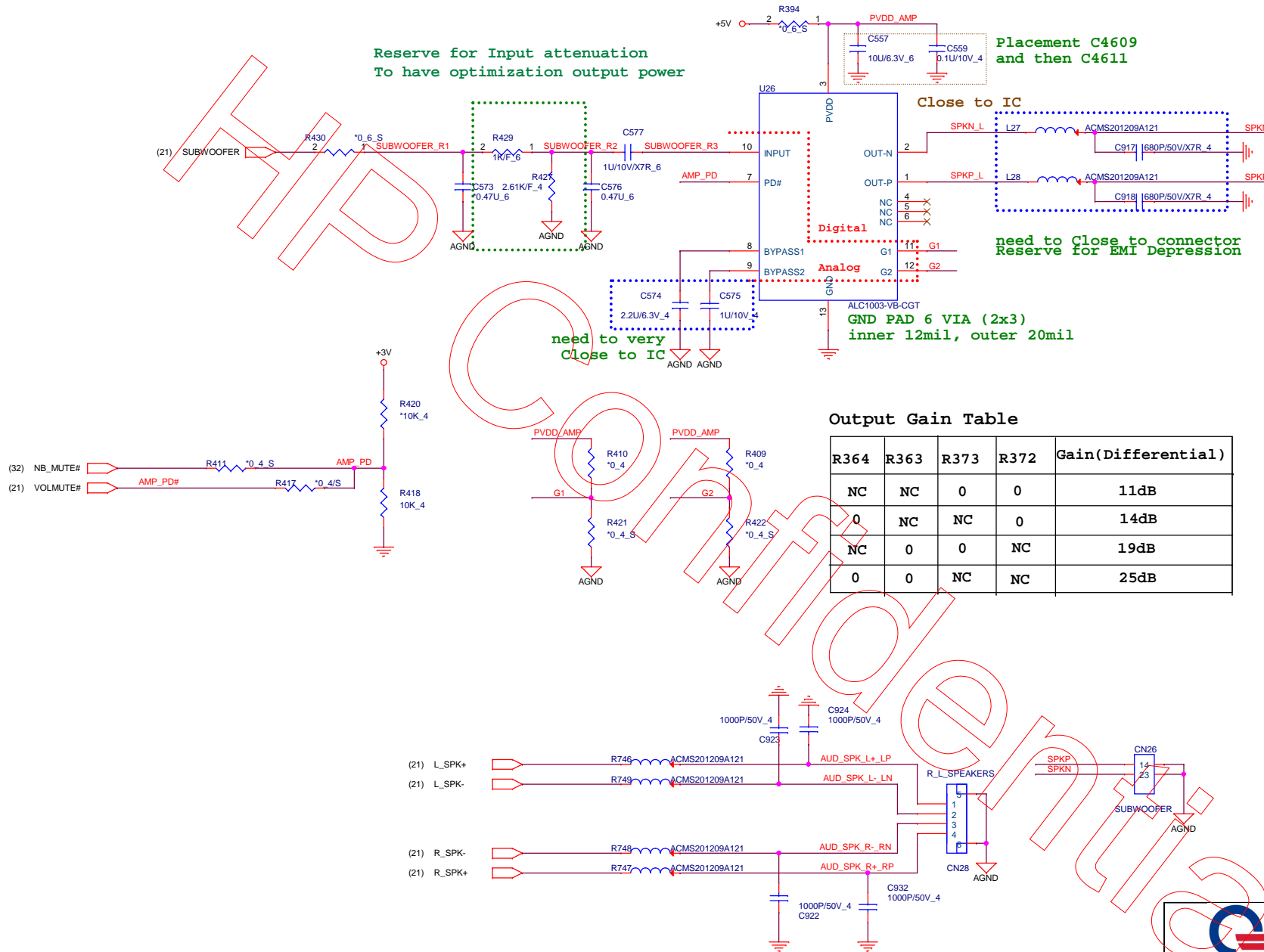
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Reserve for Input attenuation  
To have optimization output power

Placement C4609  
and then C4611

Close to IC

need to Close to connector  
Reserve for EMI Depression

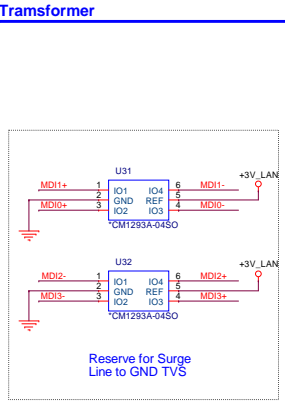
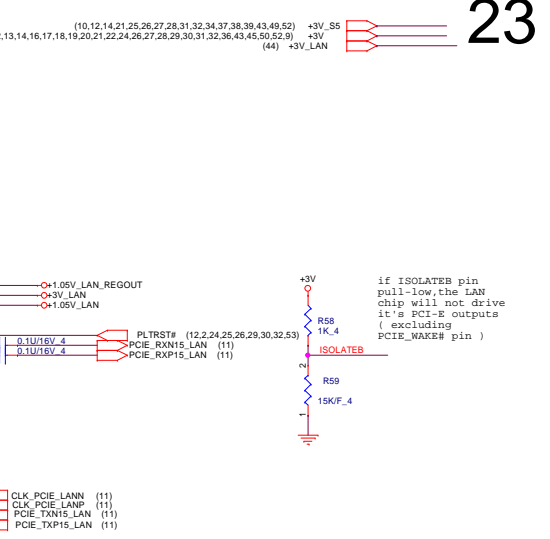
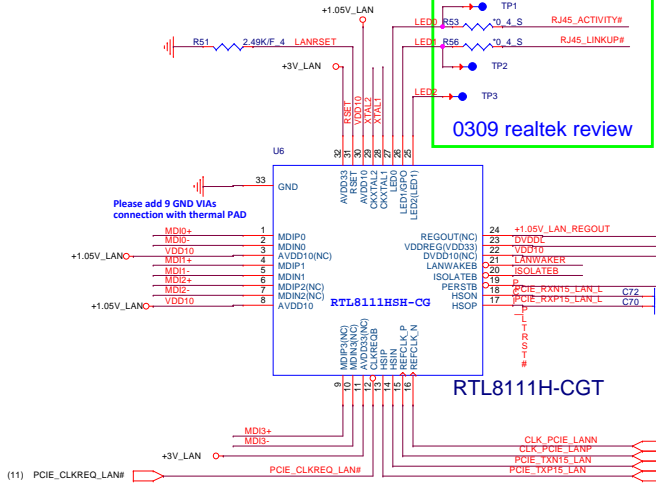
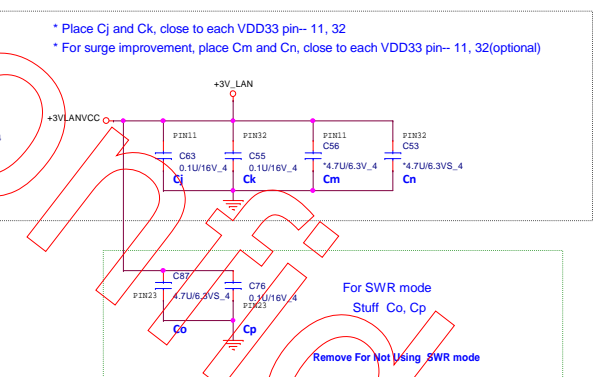
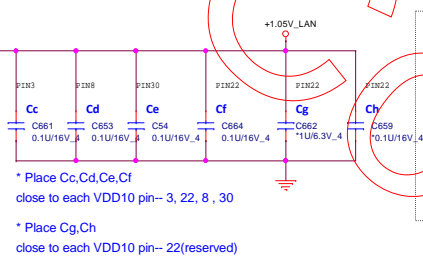
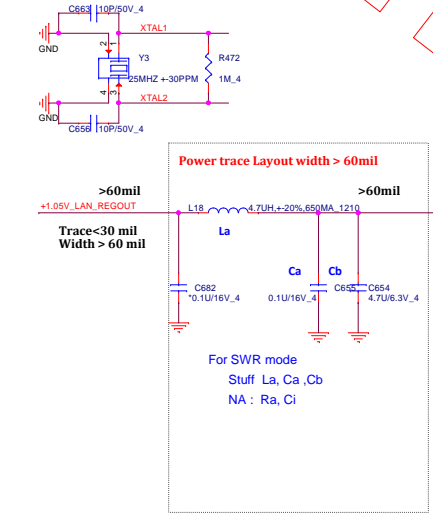
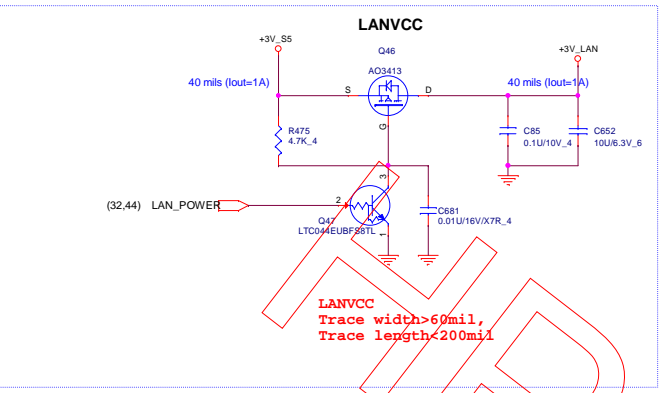
need to very  
Close to IC

GND PAD 6 VIA (2x3)  
inner 12mil, outer 20mil

Output Gain Table

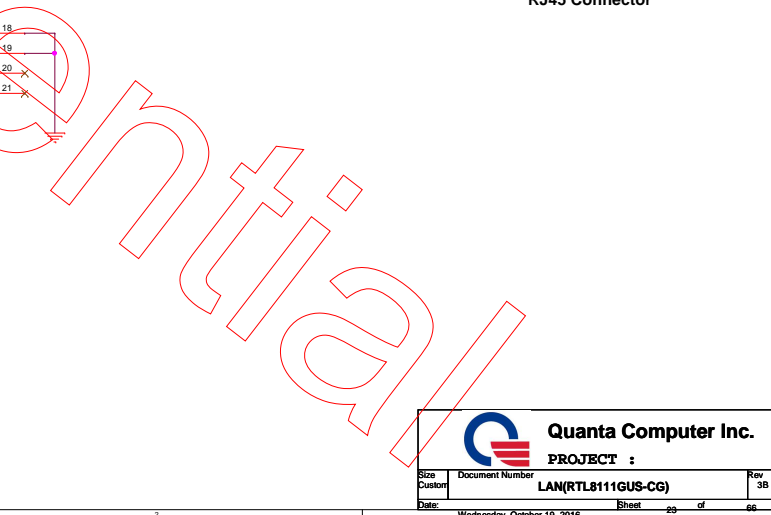
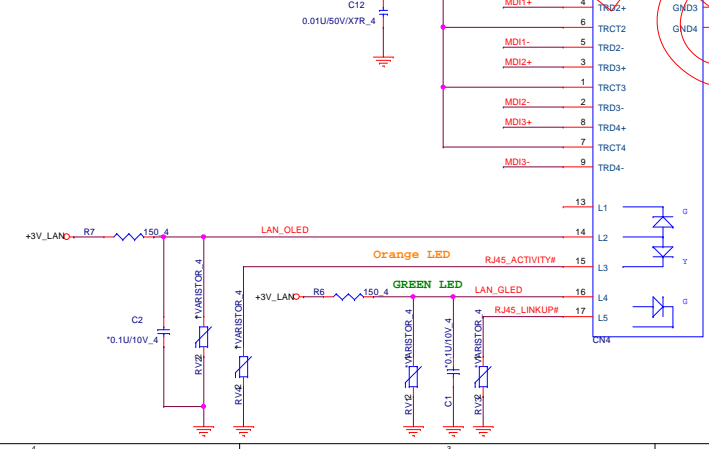
R364	R363	R373	R372	Gain(Differential)
NC	NC	0	0	11dB
0	NC	NC	0	14dB
NC	0	0	NC	19dB
0	0	NC	NC	25dB





**RJ45 Connector**

Layout: All termination  
signal should have 30  
mil trace



## SSD

(10,11,12,13,14,16,17,18,19,20,21,22,23,26,27,28,29,30,31,32,36,43,45,50,52,9)

+3V

(19,20,21,22,30,31,43,45,52,63)

+5V

24

L8H-128V2G max current: 0.844A;  
L8H-256V2G max current: 1.22A.

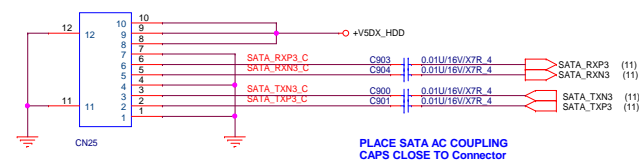
## HDD

DC Current rating: 2 A (MAX)

80 mils (lout=2A)



HDD\_CONN

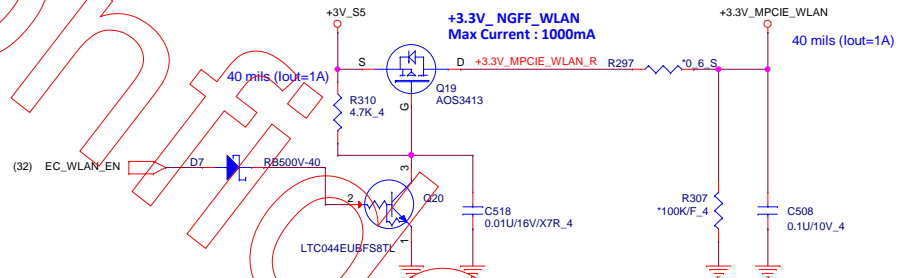
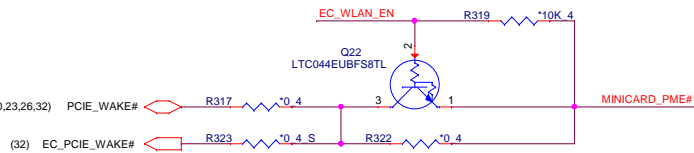
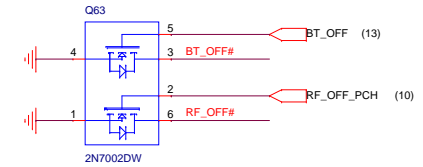
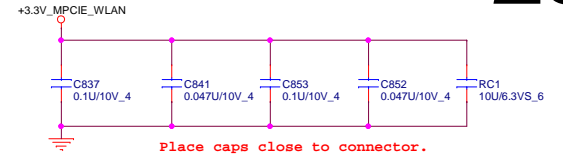
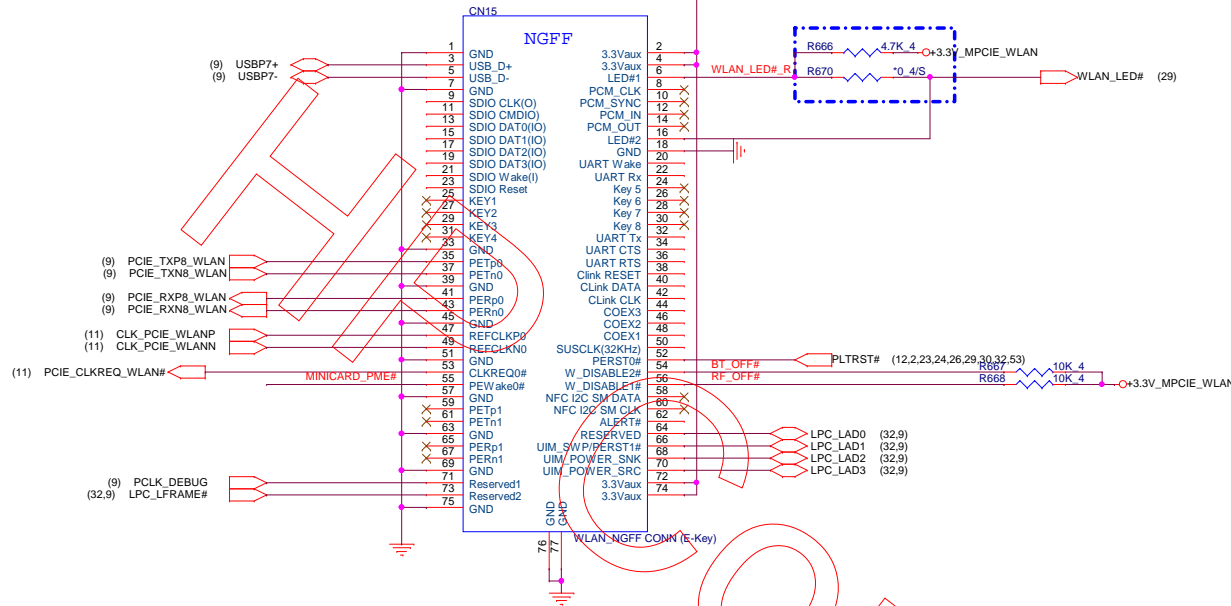
PLACE SATA AC COUPLING  
CAPS CLOSE TO Connector

		Quanta Computer Inc.	
PROJECT :		SSD mSATA X2	
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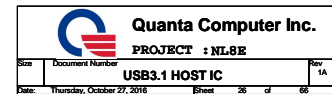
# Mini PCIE Wifi/BT connector

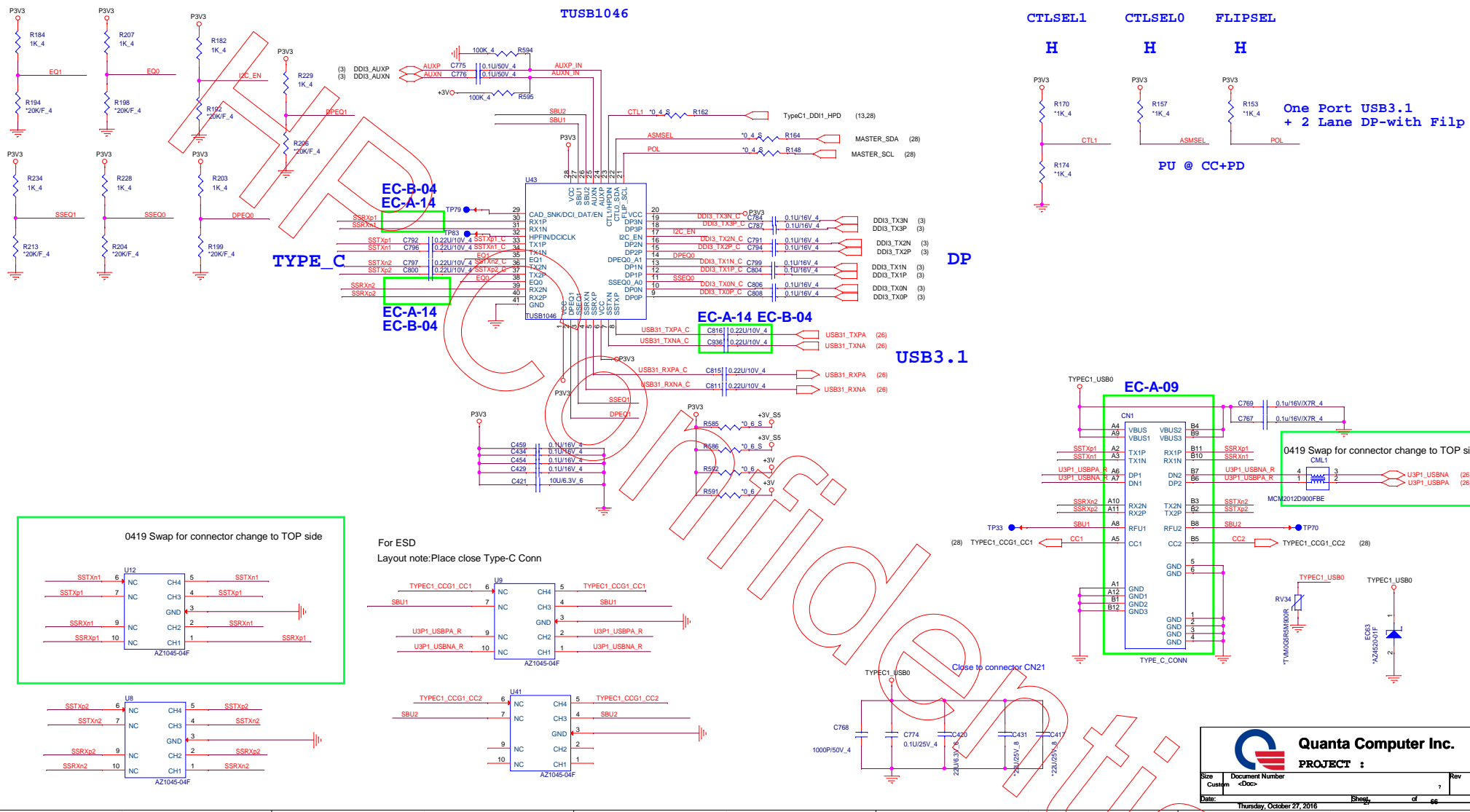
(10,12,14,21,23,26,27,28,31,32,34,37,38,39,43,49,52) +3V\_S5  
(21,38,44) +1.5V

25

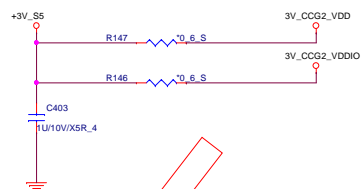


		<b>Quanta Computer Inc.</b>	
<b>PROJECT :</b>		<b>Wifi/BT MiniPCIE</b>	
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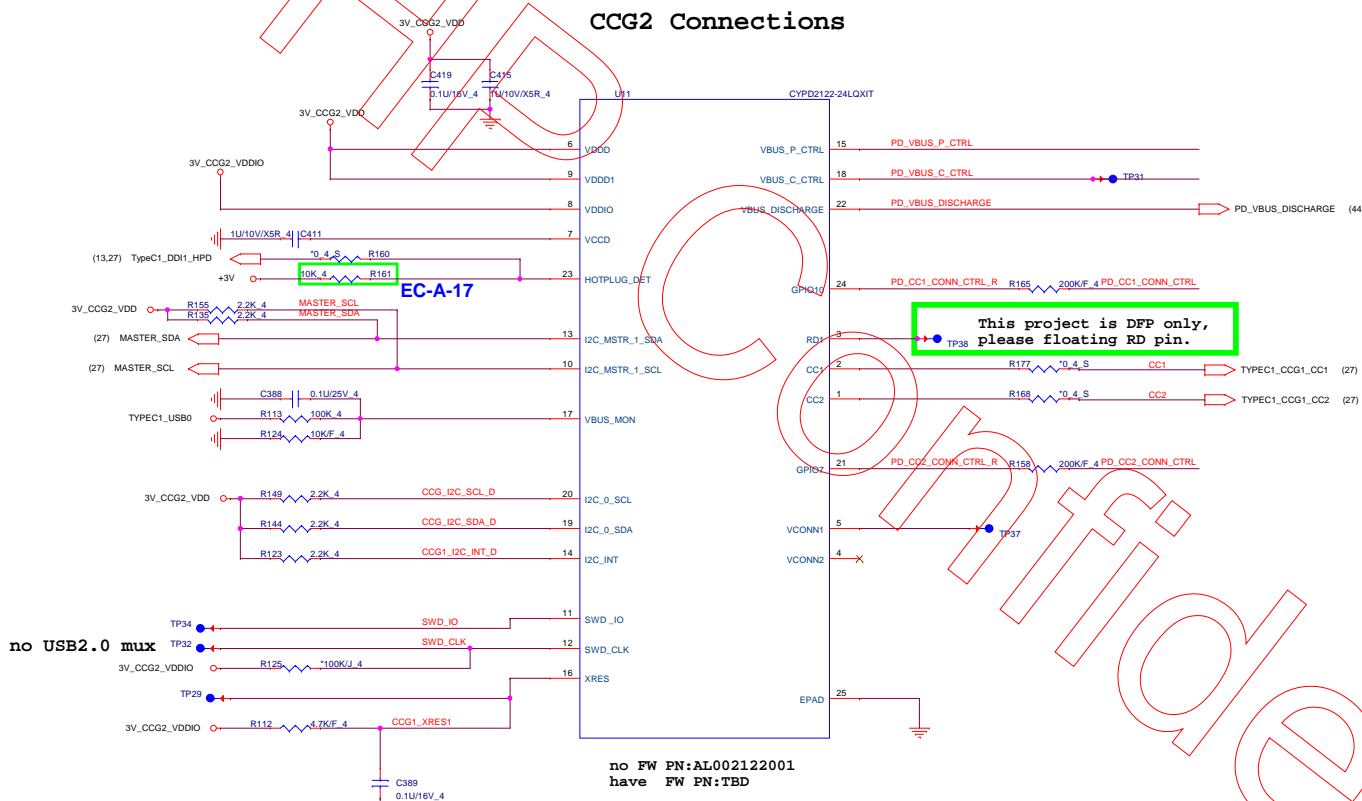




## CC+PD



## CCG2 Connections

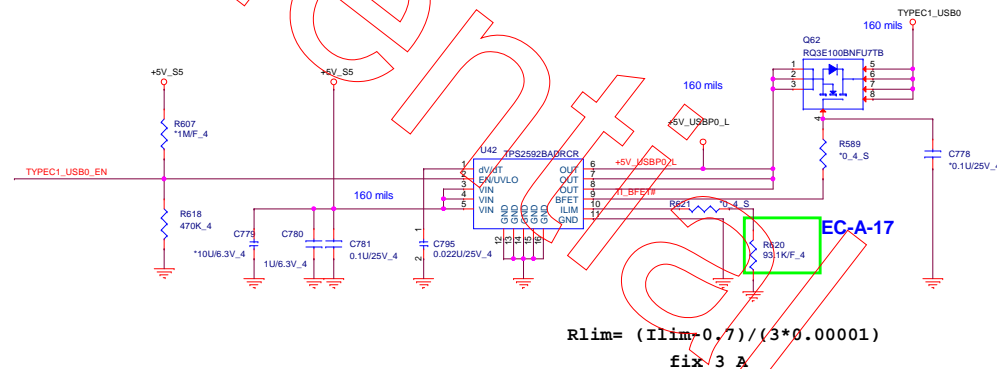
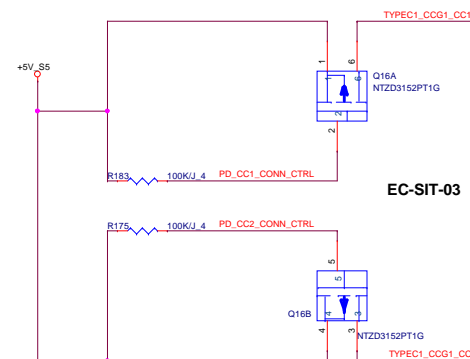


no USB2.0 mux

no FW PN:AL002122001  
have FW PN:TBD

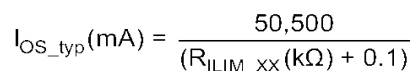
(10,26,29,34,35,36,37,39,40,41,42,43,44,45,46,47,49,50,51,52) +5V\_S5  
(10,12,14,21,23,25,26,27,31,32,34,37,38,39,43,49,52) +3V\_S5  
(27,44) TYPEC1\_USB0

## EC-SIT-03



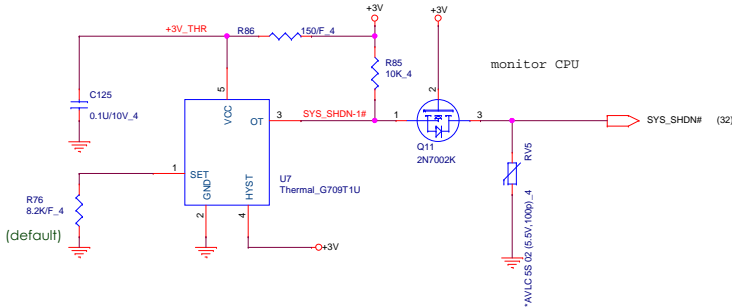
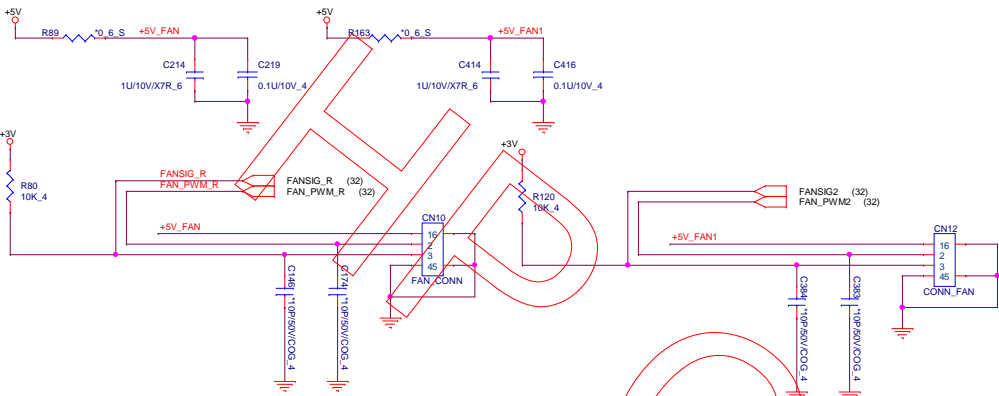
$$R_{lim} = (I_{lim} - 0.7) / (3 \times 0.00001)$$

fix 3 A

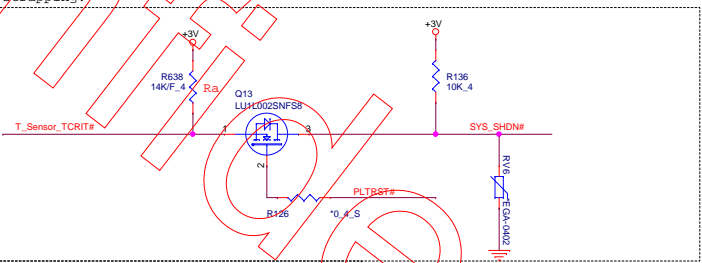
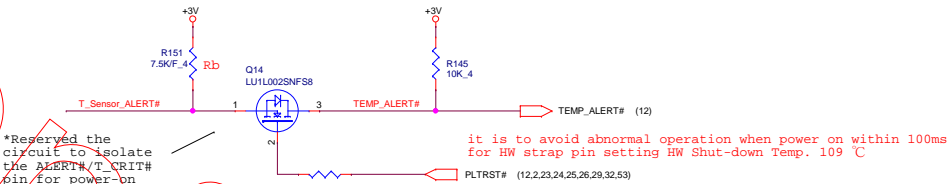
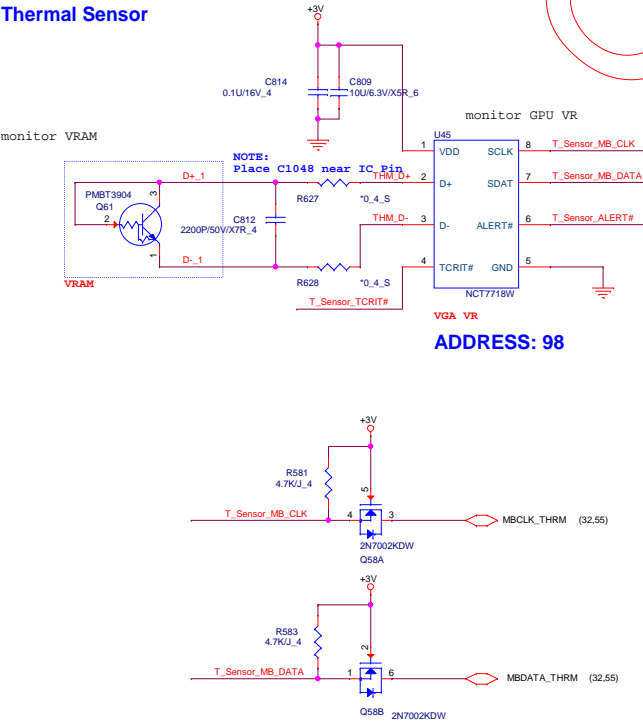
[illegible]



Thermal Sensor

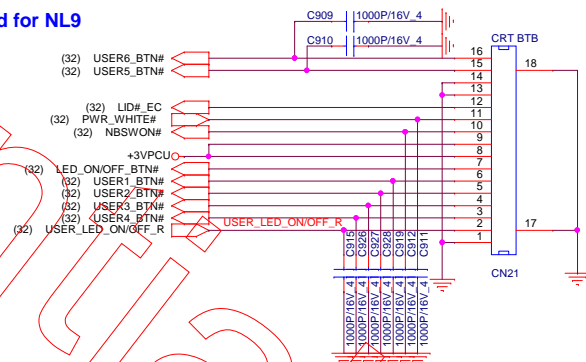
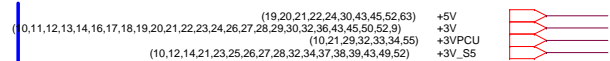


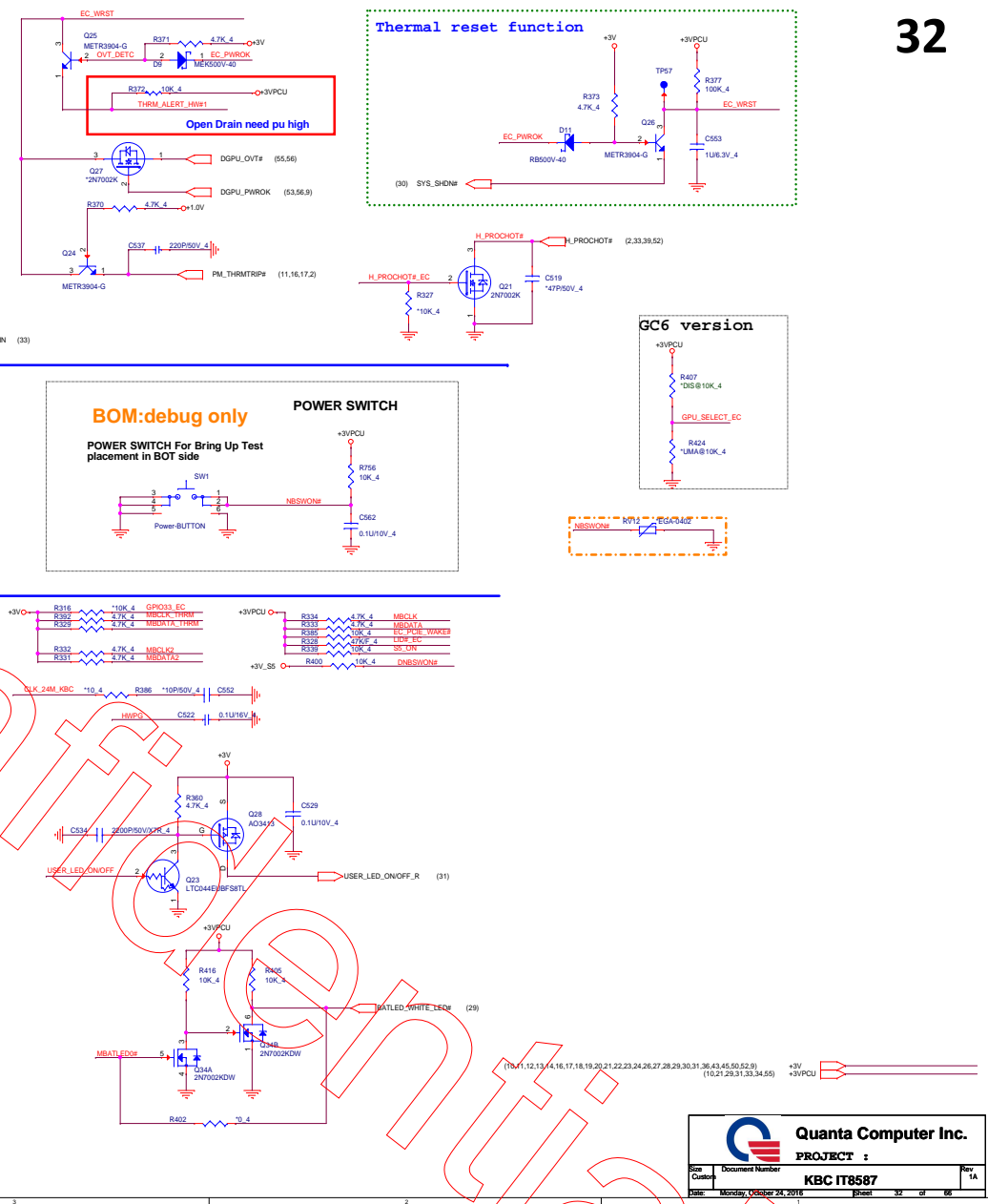
Thermal Sensor



Alert# /T_CRIT# Pull-up Resistor	
Rb	Ra
2Kohm	77°C
7.5Kohm	87°C
10.5Kohm	97°C
14Kohm	107°C
18.7Kohm	117°C
2Kohm	79°C
7.5Kohm	89°C
10.5Kohm	99°C
14Kohm	109°C
18.7Kohm	119°C
2Kohm	81°C
7.5Kohm	91°C
10.5Kohm	101°C
14Kohm	111°C
18.7Kohm	121°C
2Kohm	83°C
7.5Kohm	93°C
10.5Kohm	103°C
14Kohm	113°C
18.7Kohm	123°C
2Kohm	85°C
7.5Kohm	95°C
10.5Kohm	105°C
14Kohm	115°C
18.7Kohm	125°C

## 31





(18,34,36,38,40,41,42,47,50,52,53)  
(10,21,29,31,32,34,55)

(52) +VA  
+VIN  
+3VPCU

230W for N17E-G1 ; N17P-G1  
180W for N16E-GT (970M)  
150W for N16P-GX (960M) ; N16E-GS (965M)  
120W for N16P-GT (950M)

System Adaptor  
DC-IN

Do Not add test pad on BATDIS\_G signal

EMI request for ISN

5m ohm for 180W adaptor

Place this ZVS close to Far-Far away +VIN

Place this cap close to EC

Place this cap close to EC

For ISN

Place this cap close to EC

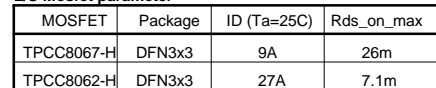
VIDCHG = 8 or 16 x (VSRN - VSRP)

Quanta Computer Inc.

PROJECT :  
Charger (BQ24780S)

Rev	Document Number	Rev
Custom		36

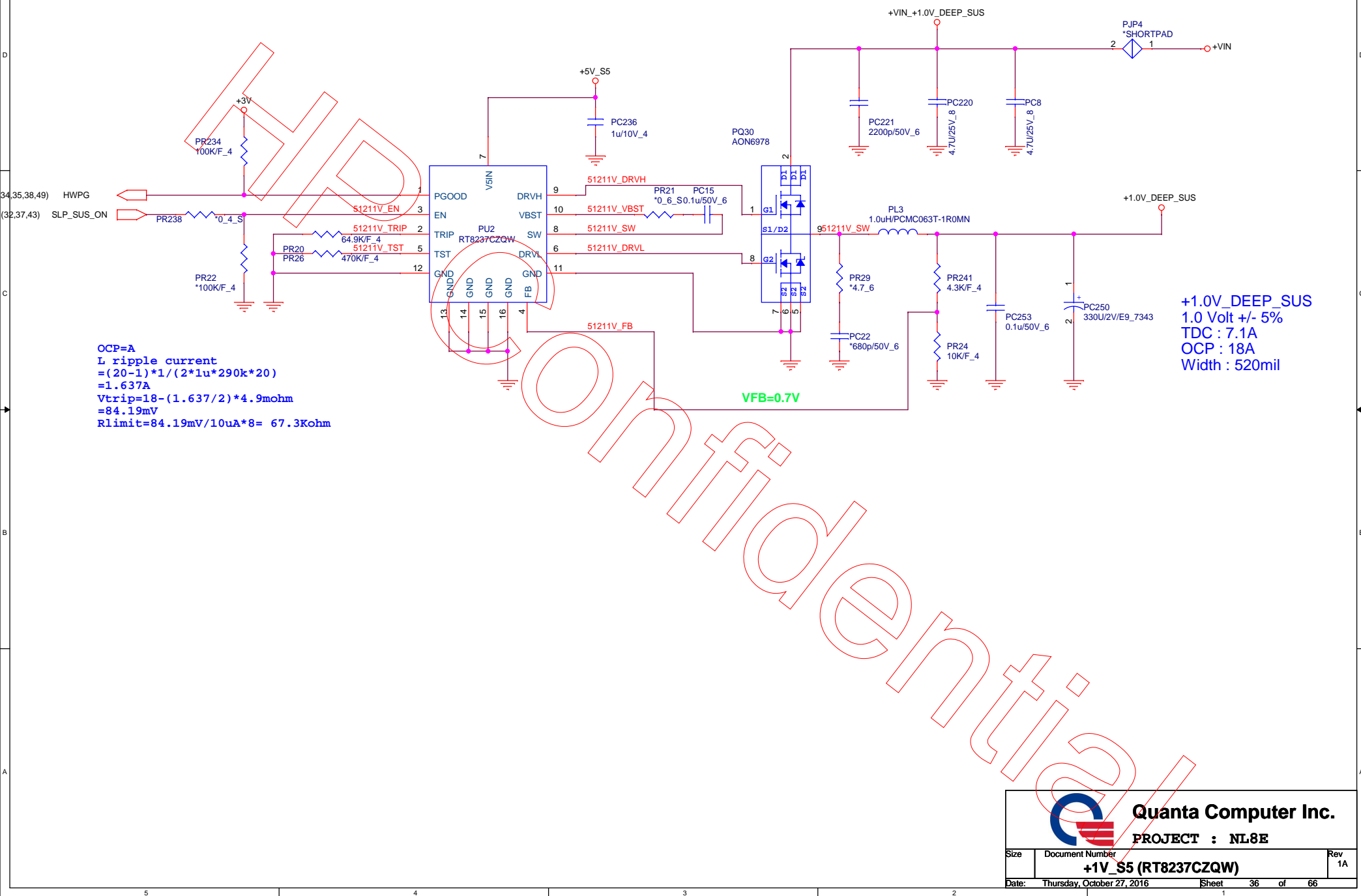
Date: Friday, October 28, 2016





~~+2.5V SUS  
2.5V<sub>olt</sub> +/- 5%  
TDC : 0.75A  
PEAK : 1A  
Width : 40mil~~

$$V_o = (0.6(R_1 + R_2)/R_2)$$



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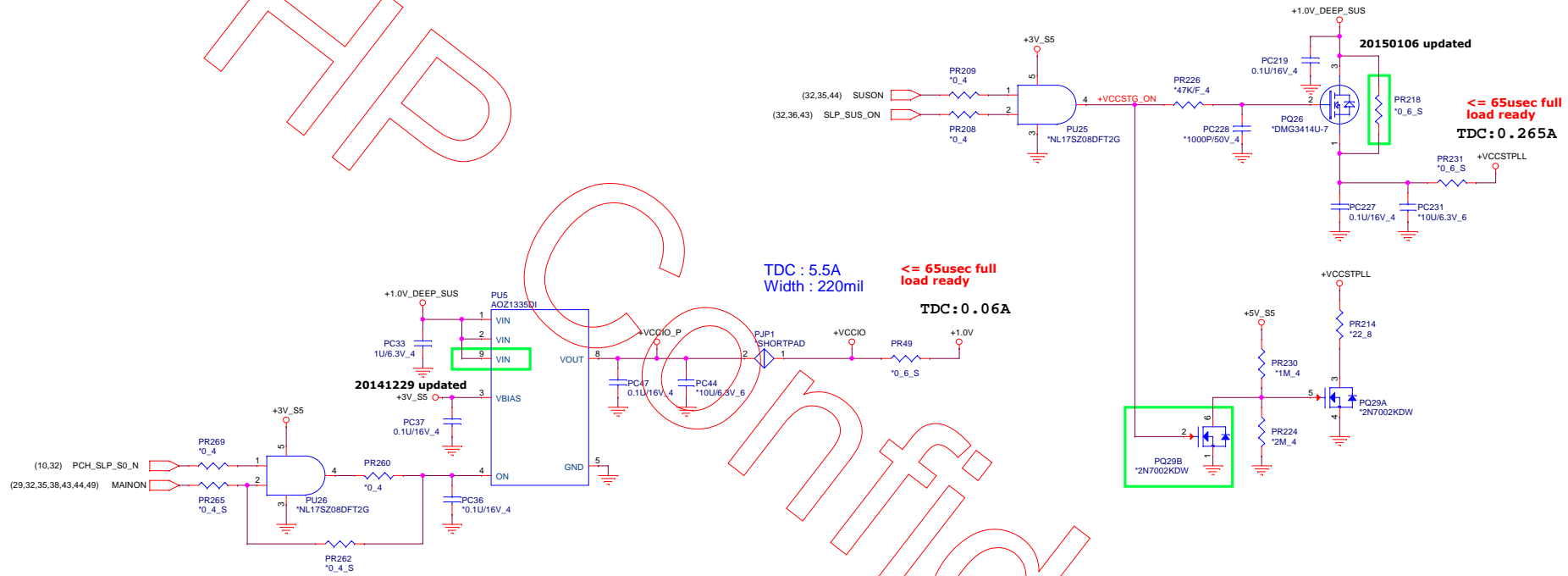
PROJECT : NL8E

Size	Document Number	Rev
	<b>+1V_S5 (RT8237CZQW)</b>	1A

Date: Thursday, October 27, 2016 Sheet 36 of 66

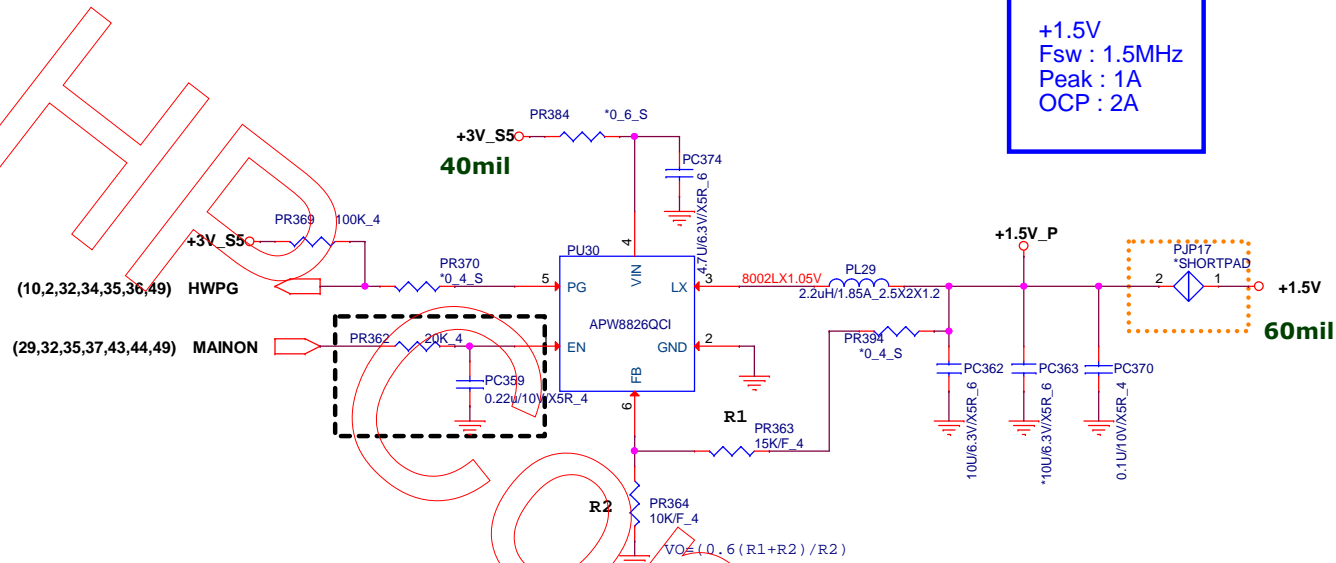


+1.0V (10,2,32,6)  
 +3V\_S5 (10,12,14,21,23,25,26,27,28,31,32,34,38,39,43,49,52)  
 +5V\_S5 (10,26,28,29,34,35,36,39,40,41,42,43,44,45,46,47,49,50,51,52)  
 +VCCIO (3,6)  
 +VCCSTPLL (11,2,6)  
 +1.0V\_DEEP\_SUS (10,11,14,36,39,44)



PROJECT : X1B-10L  
 Quanta Computer Inc.

Size Custom	Document Number +1.0V/+VCCSTPLL	Rev 1A
Date: Thursday, October 27, 2016	Sheet 37 of 66	



**Quanta Computer Inc.**

**PROJECT :**

Size	Document Number
Custom	

**+1.8V (APW8713)**

Rev  
3B

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Thursday, October 27, 2016

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Place close to VCCSA Inductor

Place close to VCORE Inductor

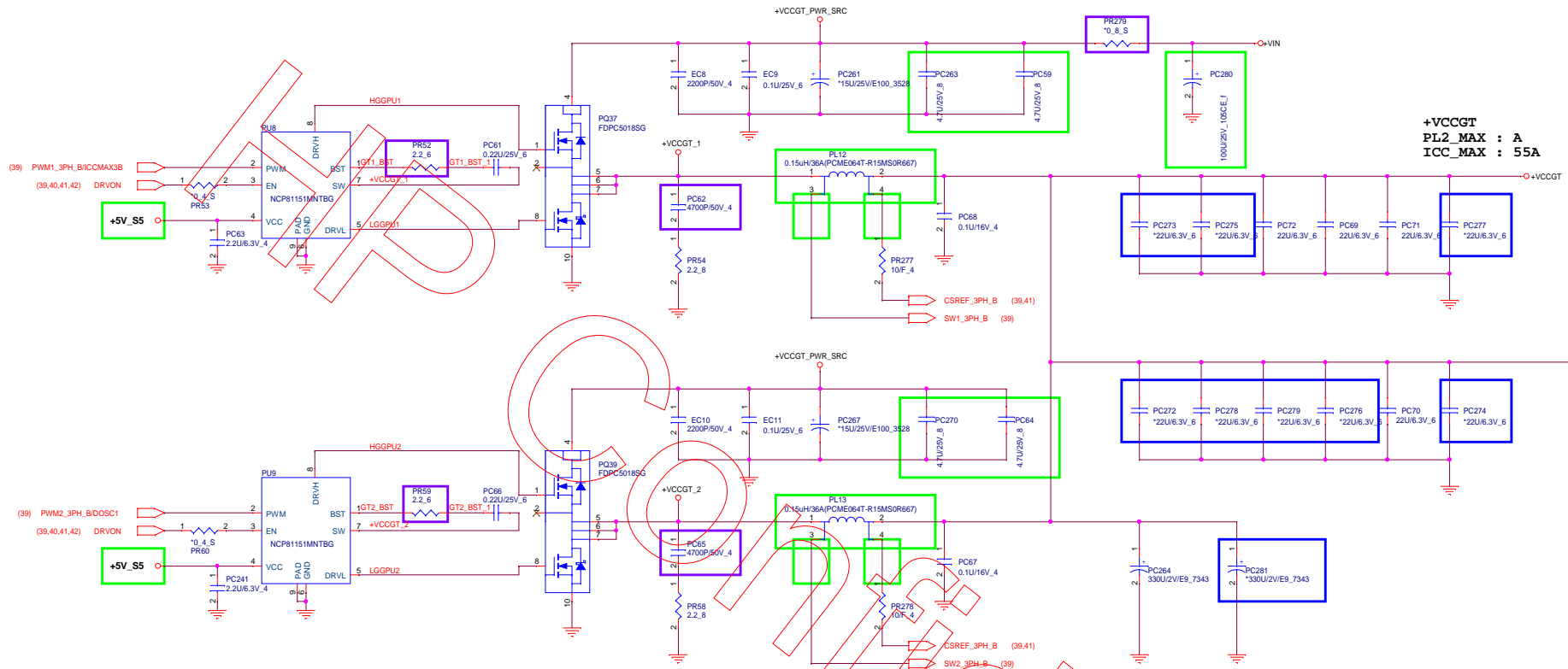
Place close to GT Inductor

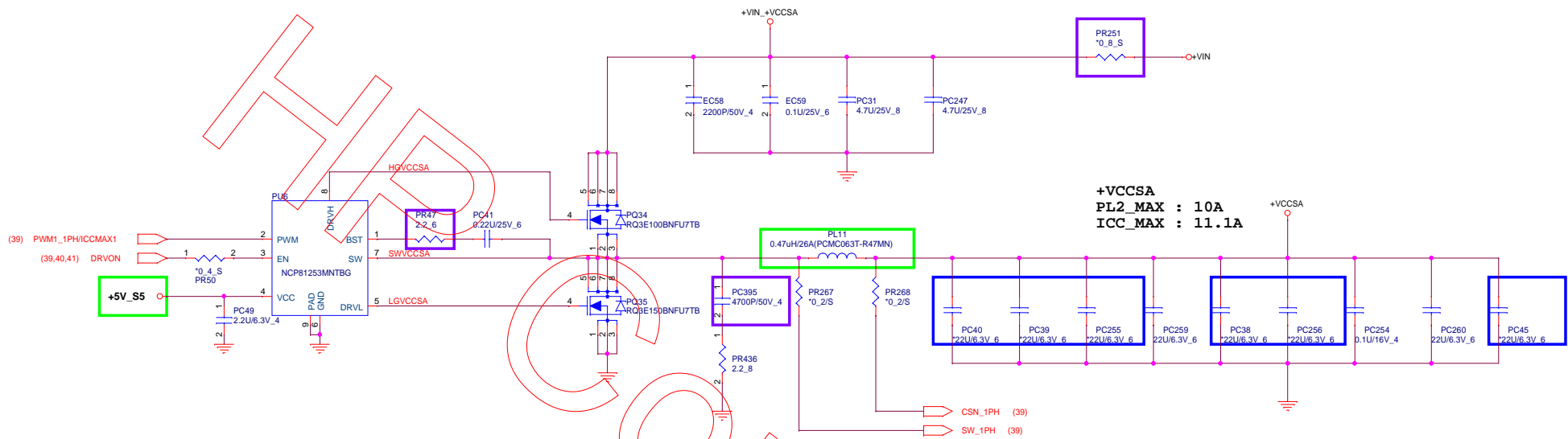
Place close to VCORE Mosfet

Place close to GT Mosfet

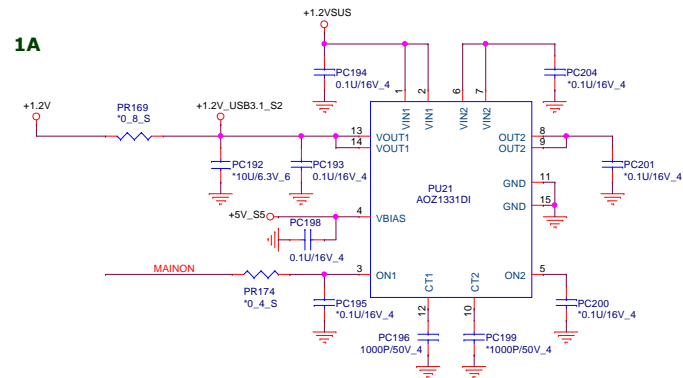
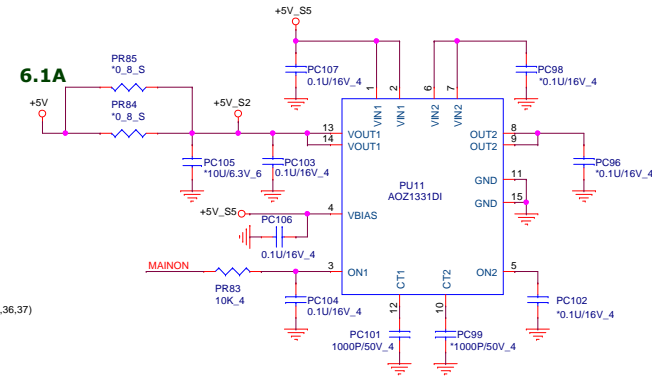
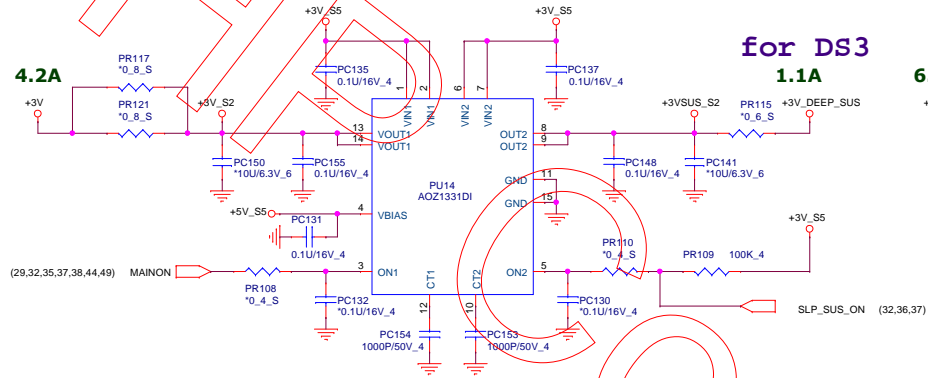
PR17  
6.06K 330W for N17E-G (CS26042FB00)  
8.695K 230W for N17E-G1; N17P-G1 (CS28662FB14)  
11.11K 180W for N16E-GT (CS31102FB11)  
13.33K 150W for N16P-GX; N16E-GS (CS31302FB19)  
16.67K 120W for N16P-GT (CS31652FB12)







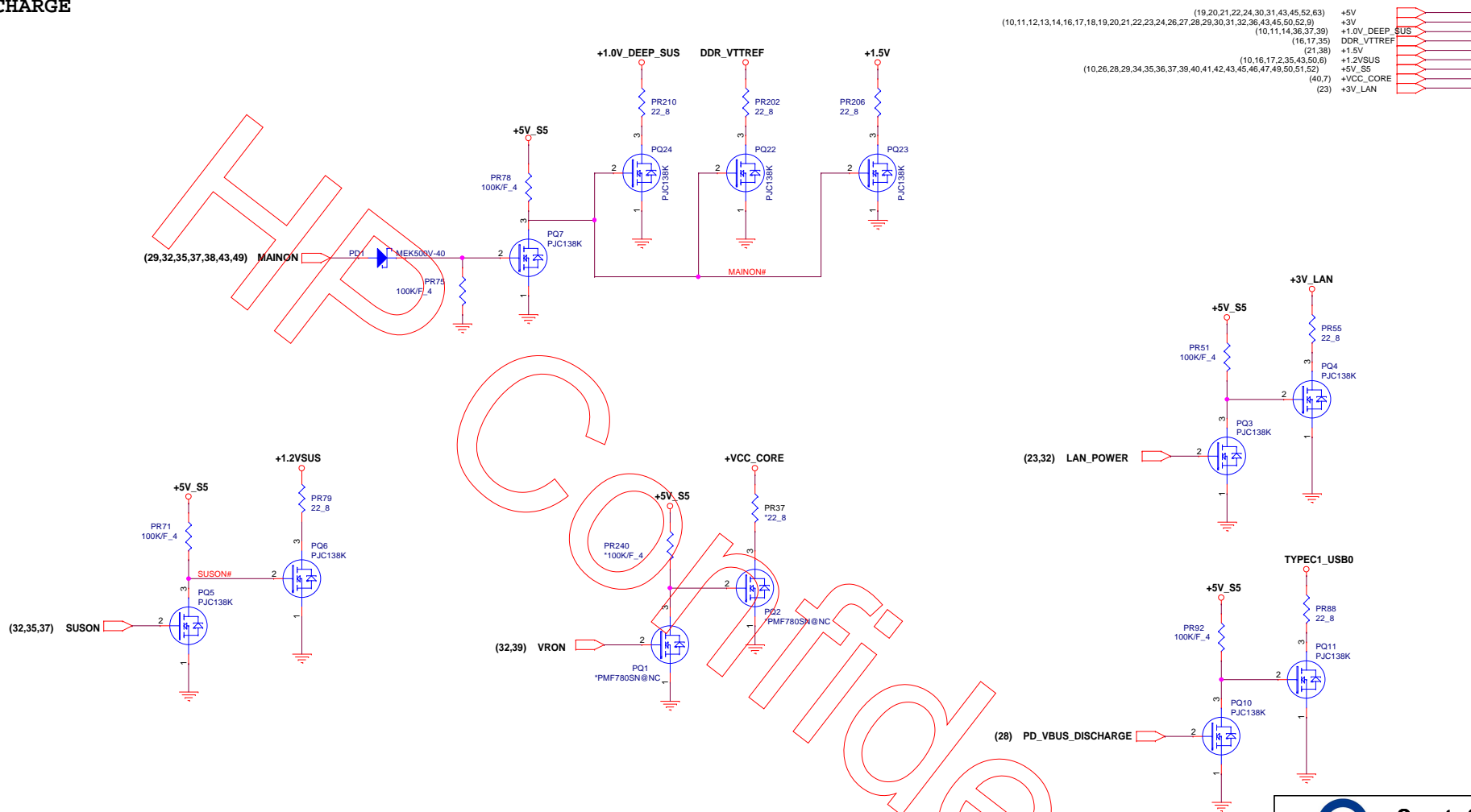
+3V (10,11,12,13,14,16,17,18,19,20,21,22,23,24,26,27,28,29,30,31,32,36,45,50,52,9)  
 +6V (19,20,21,22,24,30,31,45,52,63)  
 +3V\_S5 (10,12,14,21,23,25,26,27,28,31,32,34,37,38,39,49,52)  
 +5V\_S5 (10,26,28,29,34,35,36,37,39,40,41,42,44,45,46,47,49,50,51,52)  
 +VIN (18,33,34,35,36,39,40,41,42,47,50,52,63)

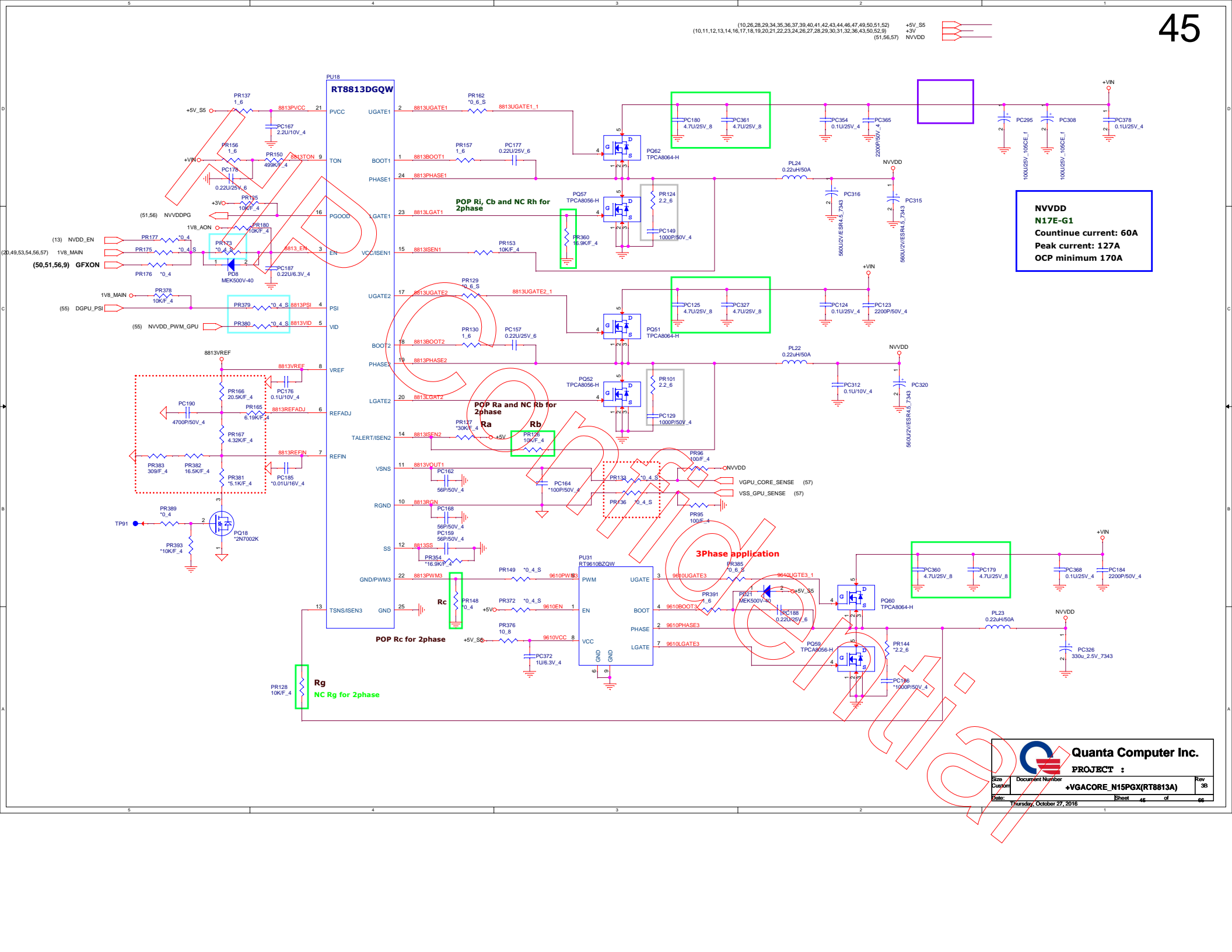


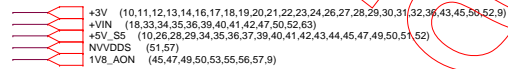


# DISCHARGE

47

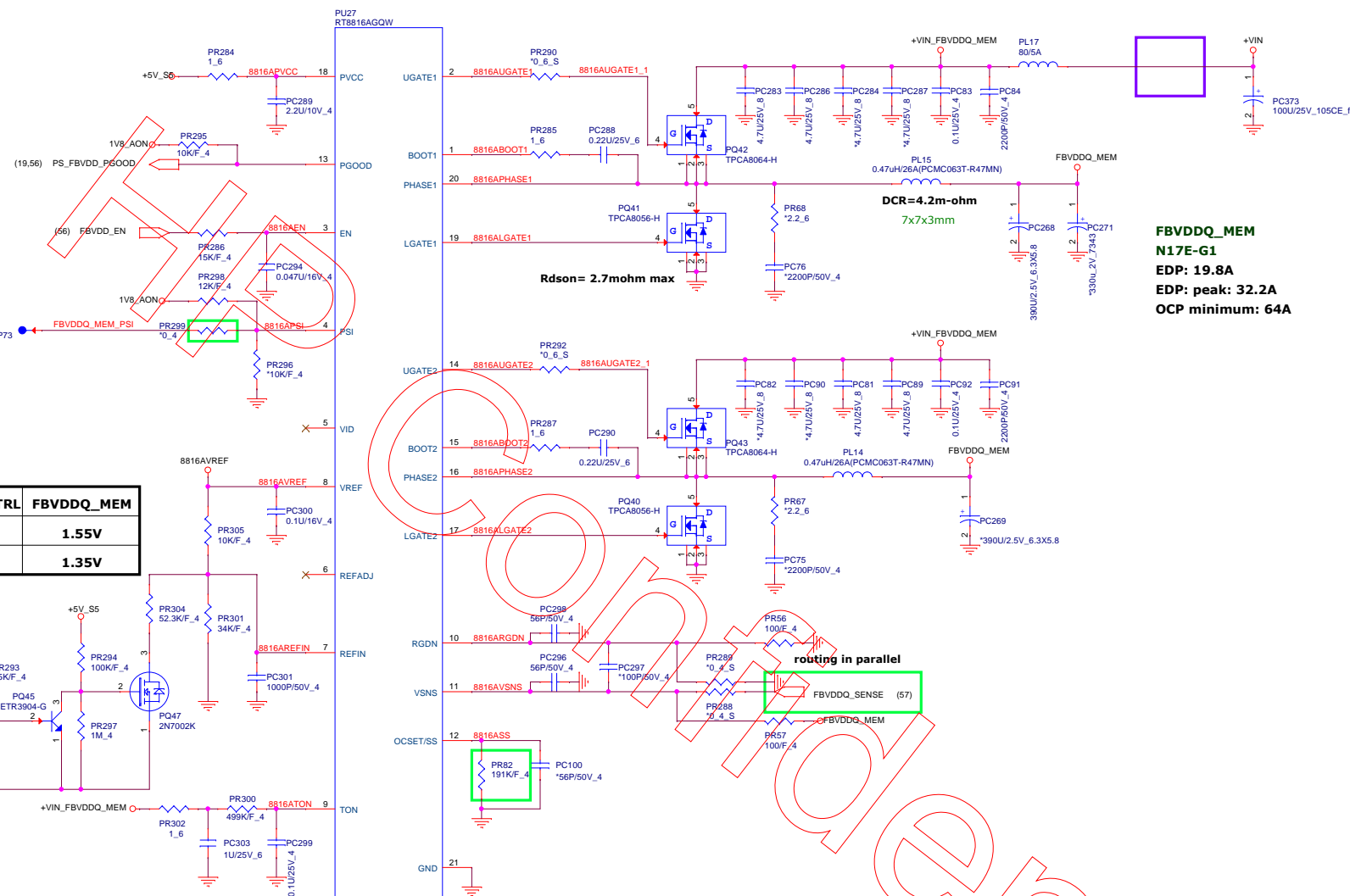






	Ra	Rb	Rc	Rd	Re	Rf
N17E-G2	NA	Stuff	232K	NA	Stuff	NA
N17E-G1	Stuff	NA	?	Stuff	NA	Stuff

9xxx




MEM_VDD_CTRL	FBVDDQ_MEM
1	1.55V
0	1.35V

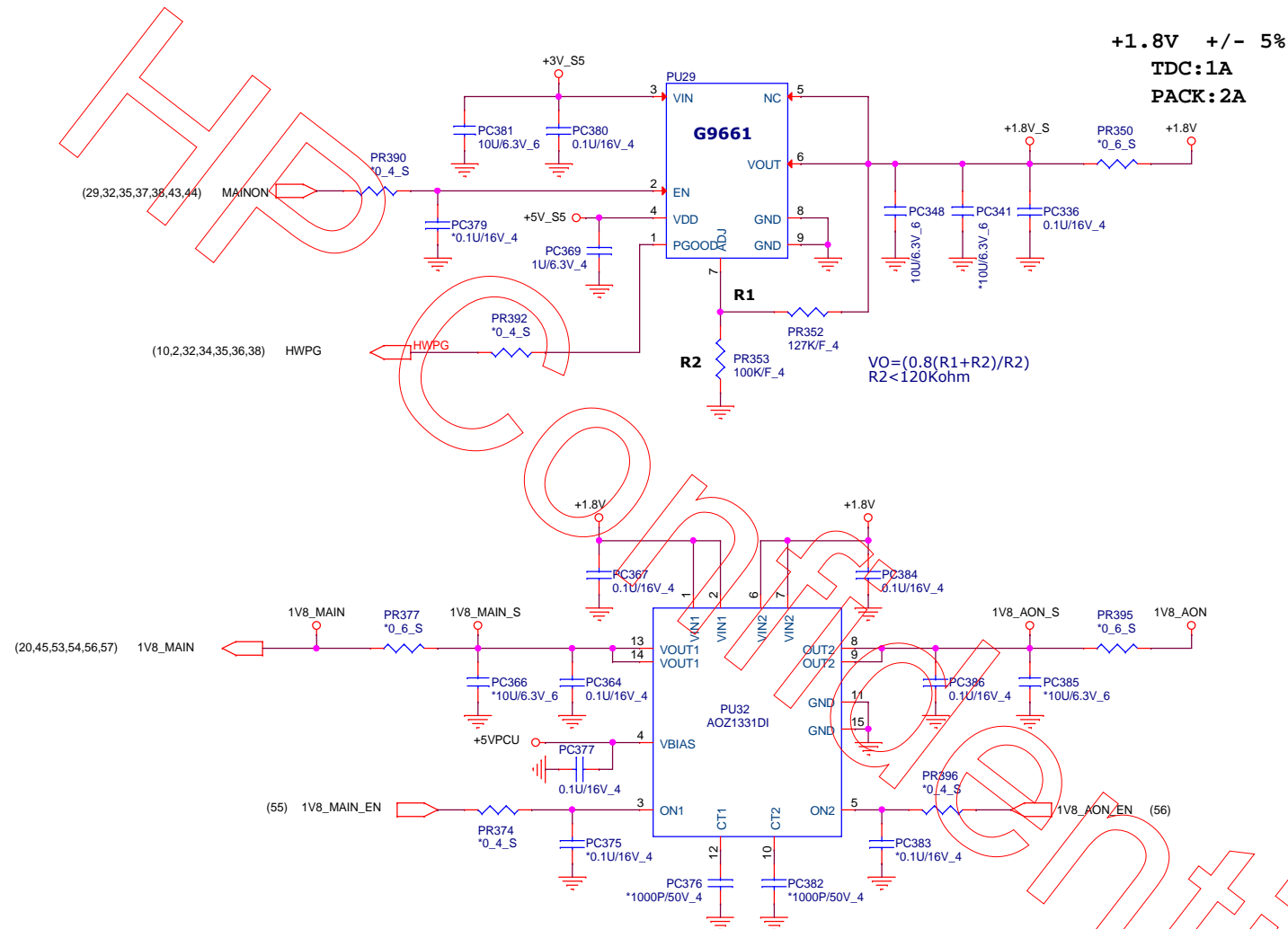
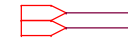
FBVDDQ\_MEM  
N17E-G1  
EDP: 19.8A  
EDP: peak: 32.2A  
OCP minimum: 64A

routing in parallel

+VIN (18,33,34,35,36,39,40,41,42,50,52,63)  
+5V\_S5 (10,26,28,29,34,35,36,37,39,40,41,42,43,44,45,46,49,50,51,52)  
FBVDDQ MEM (51,54,56,57,58,59)

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<b>Size</b> Custom	<b>Date:</b> Thursday, October 27, 2016	<b>Sheet</b> 48 <b>of</b> 66

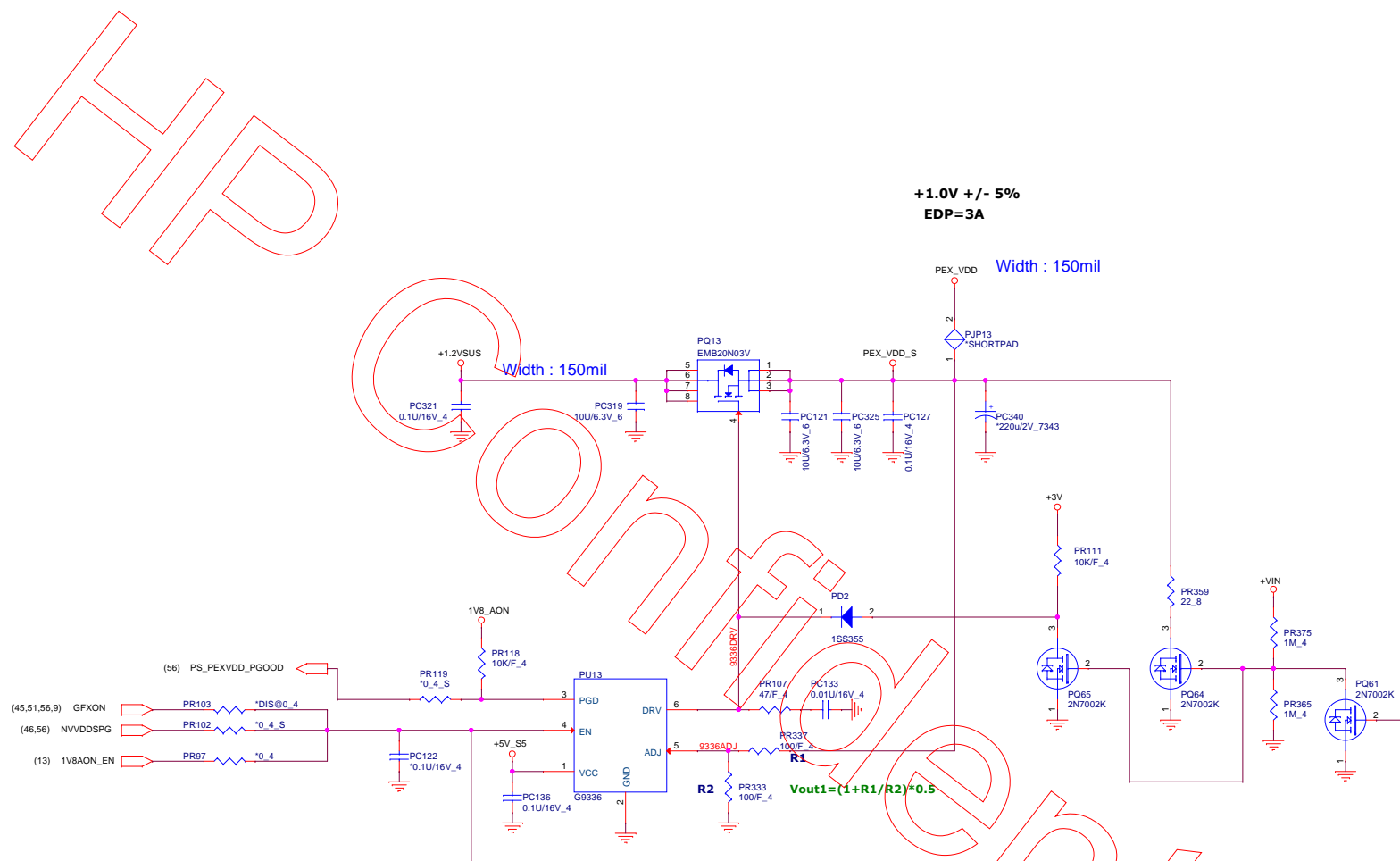


Quanta Computer Inc.

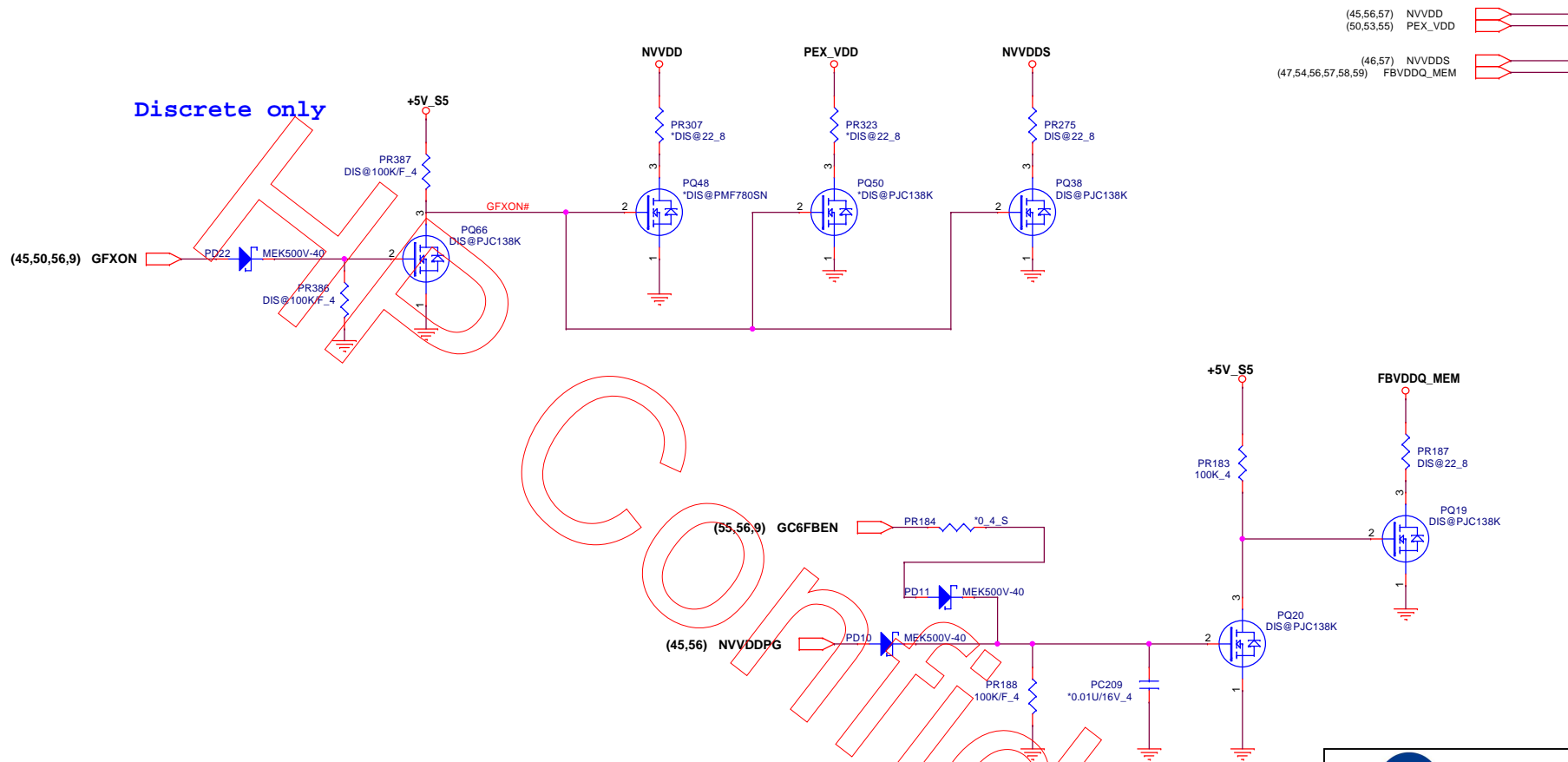
PROJECT :


Size Custom Document Number **+1.8V (APW8713)** Rev 38

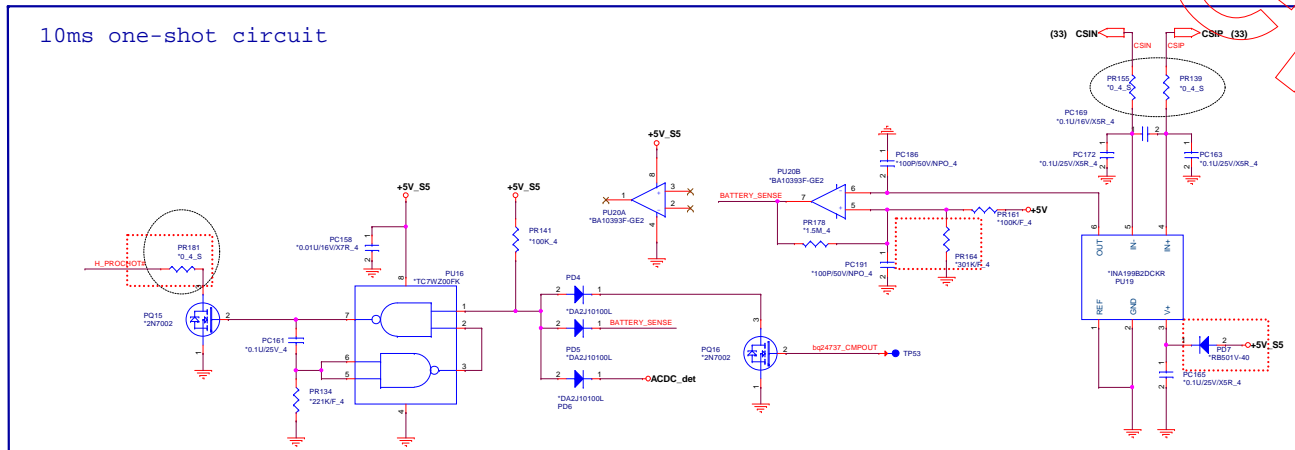
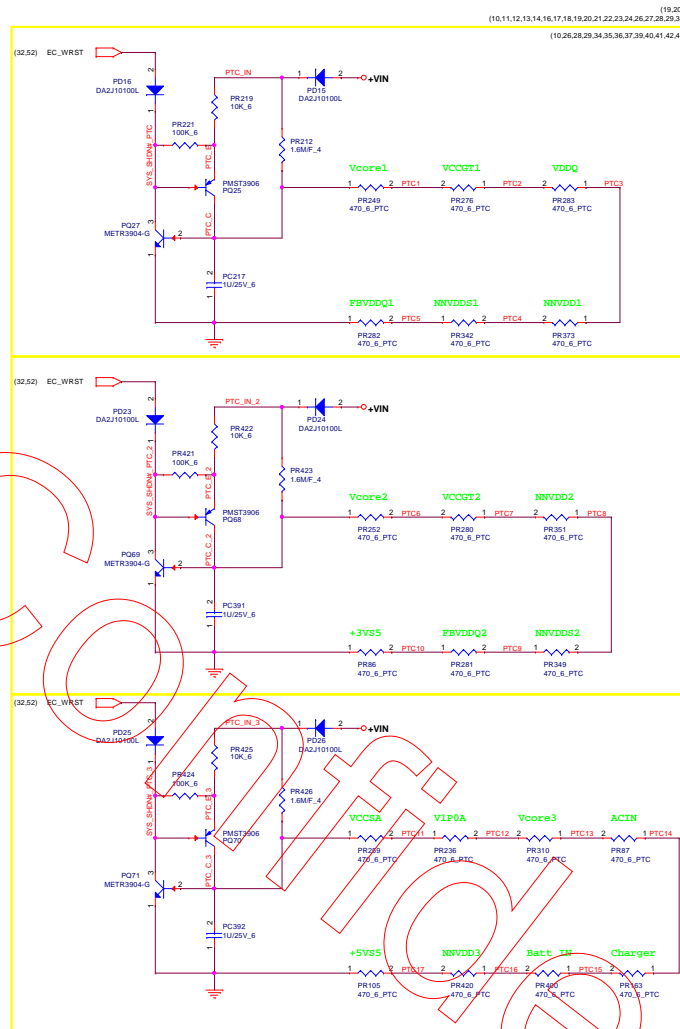
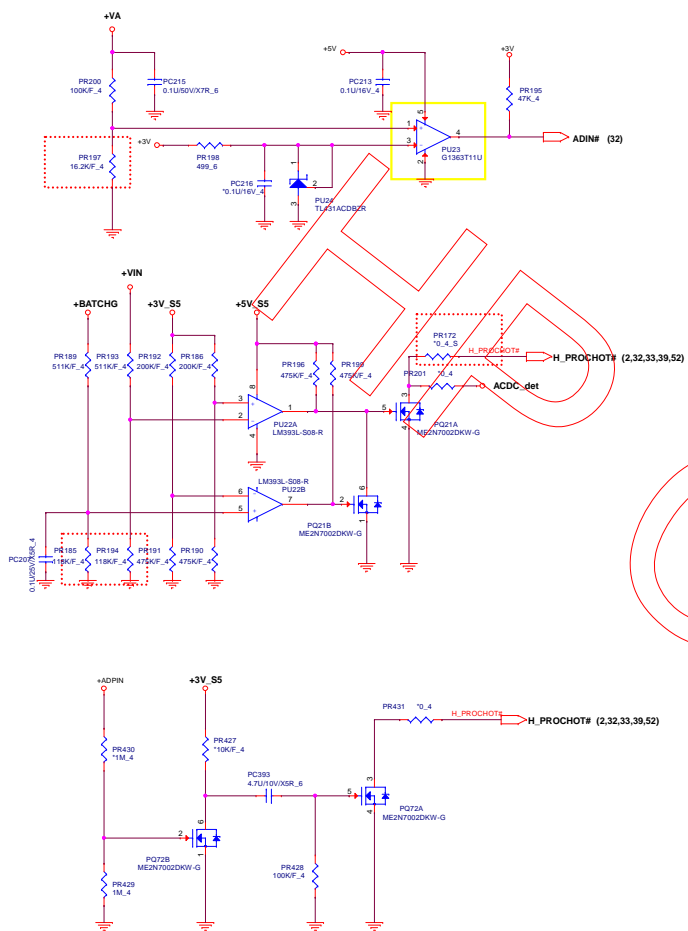
Date: Thursday, October 27, 2016 Sheet 49 of 66

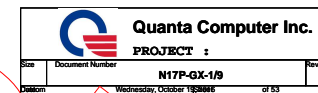






 <b>Quanta Computer Inc.</b>		
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STRAP[2:0] VRAM Table for N17P-G1 GDDR5 Recommended Memories

STRAP[2:0]	DESCRIPTION	Vendor	Vendor Part	TOP P/N	GB P/N
001	GDDR5 2048x128 G1a	Samsung	S406322270-0001	TOP	Meo000100
002	GDDR5 2048x128 G1a	Hynix	H5G8224070-0002	TOP	Meo000200

Table 5.3 RAMCFG

STRAP2	STRAP1	STRAP0	RAMCFG Setting Number (see Memory I/VL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	M	10 (0x000A)
L	M	H	11 (0x000B)
M	L	L	12 (0x000C)
M	L	M	13 (0x000D)

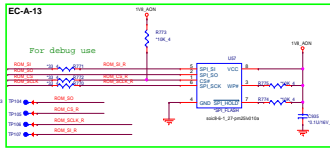


Table 5.5 SORX\_EXPOSED Strap Enablement for Down Designs

Row Index	ROM_CS	ROM_SI	ROM_SCLK	SOR1_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR2_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	ENABLED	ENABLED	ENABLED
13	L	H	L	ENABLED	ENABLED	ENABLED	ENABLED	ENABLED	ENABLED
12	L	H	H	ENABLED	ENABLED	ENABLED	ENABLED	ENABLED	ENABLED
11	H	L	L	ENABLED	ENABLED	ENABLED	ENABLED	ENABLED	ENABLED
10	H	L	H	ENABLED	ENABLED	ENABLED	ENABLED	ENABLED	ENABLED
9	H	H	L	ENABLED	ENABLED	ENABLED	ENABLED	ENABLED	ENABLED
8	H	H	H	ENABLED	ENABLED	ENABLED	ENABLED	ENABLED	ENABLED
0	M	M	M	disabled	disabled	disabled	disabled	disabled	disabled
M	M	M	M	disabled	disabled	disabled	disabled	disabled	disabled

Note: The tertiary strap pins listed in the Strap Pins column should be pulled to one of three voltage levels: "L" means Low level (0V), "H" means High level (0.9V), "M" means High level (1.8V).

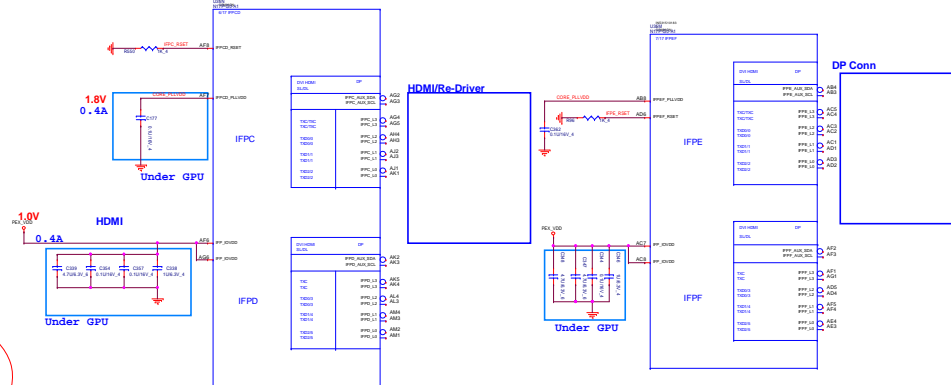
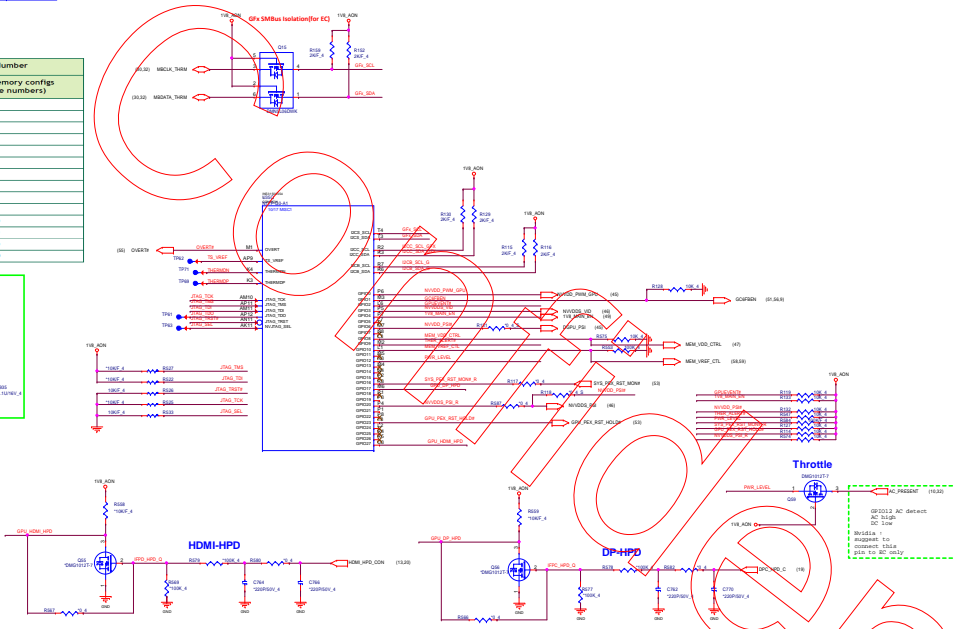


Table 14.1 GPIO Descriptions for GB4C-128 Packages

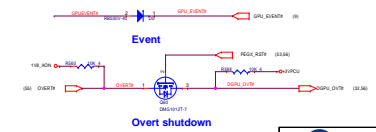
GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	AVDD_PWM_VID	O	PWM Output to control NVDD	0 to 1V8 PWM output
GPIO1	GC6M: GC6_FB_EN	O	FB Enable for GC6 2.1	Open Source 10 KΩ pull-down

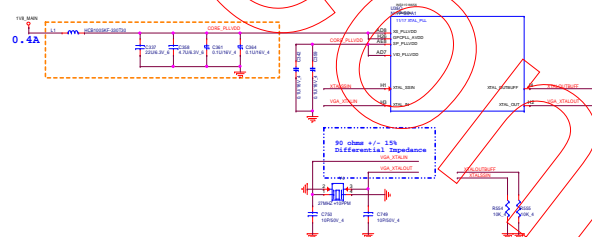
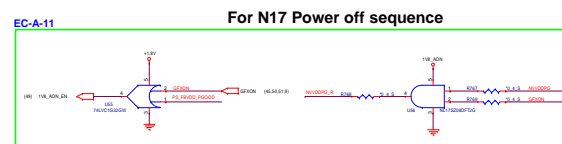
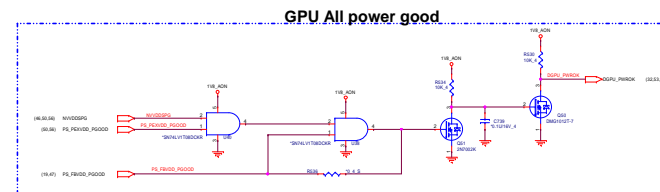
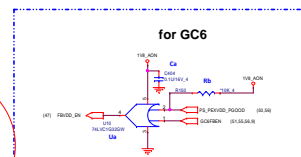
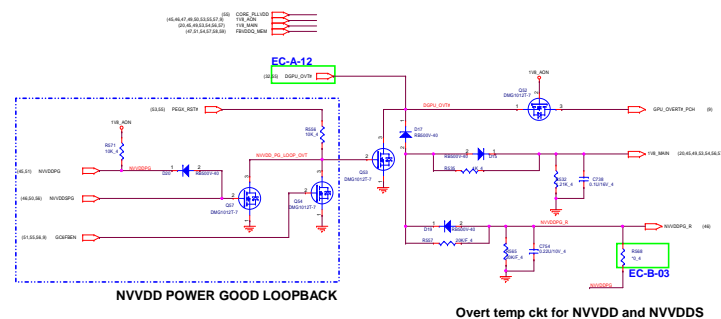
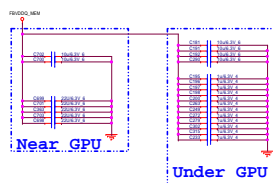
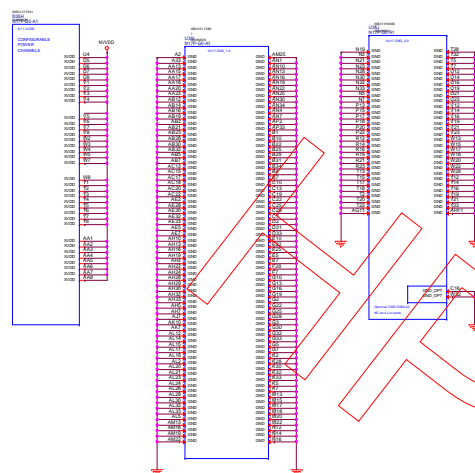
Table 14.1 GPIO Descriptions for GB4C-128 Packages (Continued)

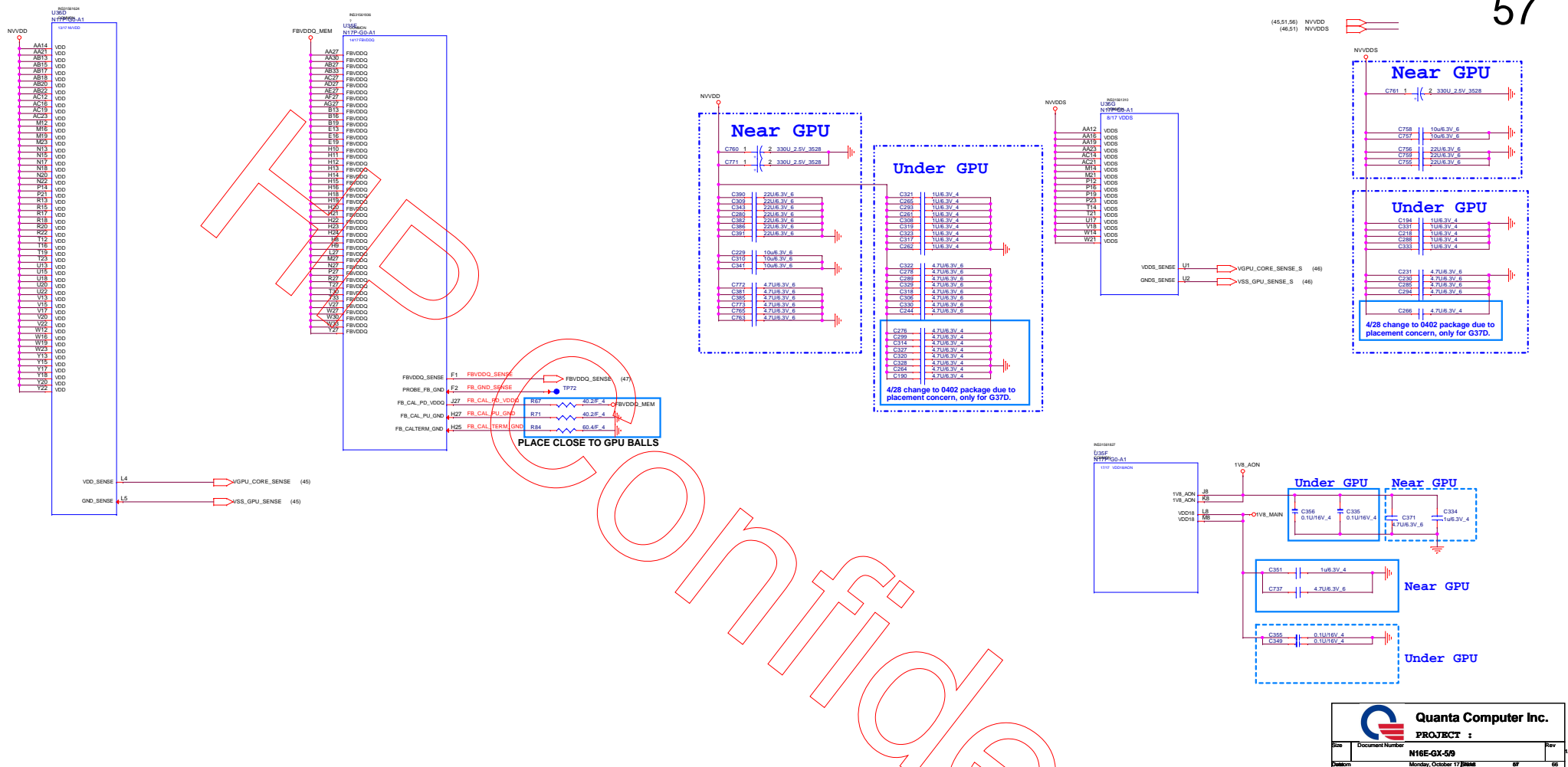
GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO2	GPU_RESET	I	GPU Reset	100 KΩ pull-up to 1V8
GPIO3	GPU_RESET_N	I	GPU Reset	100 KΩ pull-up to 1V8
GPIO4	GPU_RESET_N	I	GPU Reset	100 KΩ pull-up to 1V8
GPIO5	GPU_RESET_N	I	GPU Reset	100 KΩ pull-up to 1V8
GPIO6	GPU_RESET_N	I	GPU Reset	100 KΩ pull-up to 1V8
GPIO7	GPU_RESET_N	I	GPU Reset	100 KΩ pull-up to 1V8
GPIO8	GPU_RESET_N	I	GPU Reset	100 KΩ pull-up to 1V8
GPIO9	GPU_RESET_N	I	GPU Reset	100 KΩ pull-up to 1V8
GPIO10	GPU_RESET_N	I	GPU Reset	100 KΩ pull-up to 1V8
GPIO11	GPU_RESET_N	I	GPU Reset	100 KΩ pull-up to 1V8
GPIO12	GPU_RESET_N	I	GPU Reset	100 KΩ pull-up to 1V8
GPIO13	GPU_RESET_N	I	GPU Reset	100 KΩ pull-up to 1V8
GPIO14	GPU_RESET_N	I	GPU Reset	100 KΩ pull-up to 1V8
GPIO15	GPU_RESET_N	I	GPU Reset	100 KΩ pull-up to 1V8
GPIO16	GPU_RESET_N	I	GPU Reset	100 KΩ pull-up to 1V8
GPIO17	GPU_RESET_N	I	GPU Reset	100 KΩ pull-up to 1V8



GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO18	GPU_RESET_N	I	GPU Reset	100 KΩ pull-up to 1V8
GPIO19	GPU_RESET_N	I	GPU Reset	100 KΩ pull-up to 1V8
GPIO20	GPU_RESET_N	I	GPU Reset	100 KΩ pull-up to 1V8
GPIO21	GPU_RESET_N	I	GPU Reset	100 KΩ pull-up to 1V8
GPIO22	GPU_RESET_N	I	GPU Reset	100 KΩ pull-up to 1V8
GPIO23	GPU_RESET_N	I	GPU Reset	100 KΩ pull-up to 1V8
GPIO24	GPU_RESET_N	I	GPU Reset	100 KΩ pull-up to 1V8
GPIO25	GPU_RESET_N	I	GPU Reset	100 KΩ pull-up to 1V8
GPIO26	GPU_RESET_N	I	GPU Reset	100 KΩ pull-up to 1V8
GPIO27	GPU_RESET_N	I	GPU Reset	100 KΩ pull-up to 1V8









**CHANNEL A: 1024MB GDDR5x32**

(47,51,54,56,57,59) FBVDDQ\_MEM 

Channel A  
<0-31>

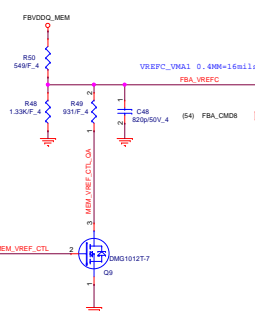
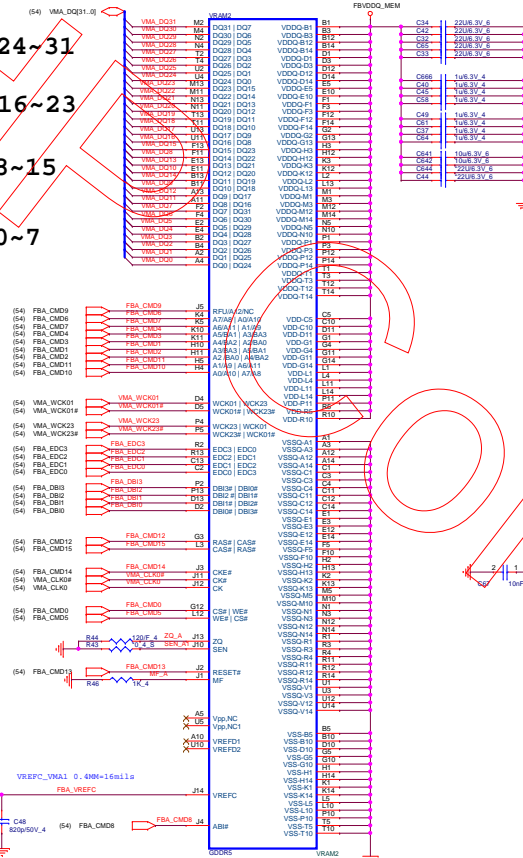
MF=0 Non-mirrored

~~QD24~31~~

~~QD16~23~~

~~QD8~15~~

QD0~7



(55,59) MEM\_VREF\_CTL  MEM\_VREF\_CTL 2  DMG1012T-7

Channel A  
<32-63>

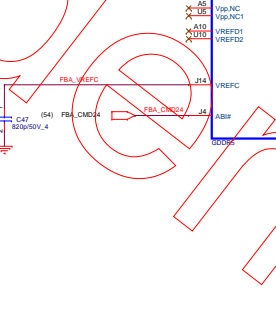
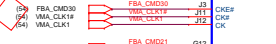
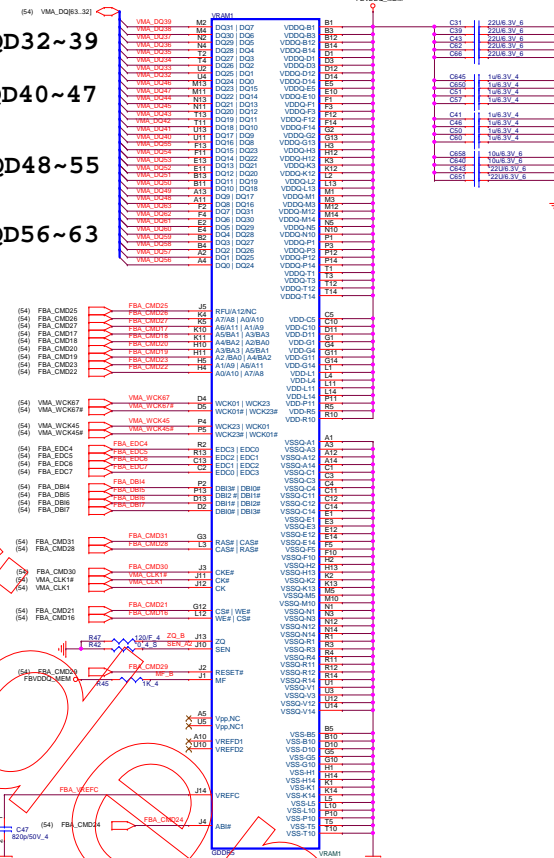
MF=1 mirrored

QD32~39

QD40~47

QD48~55

QD56~63

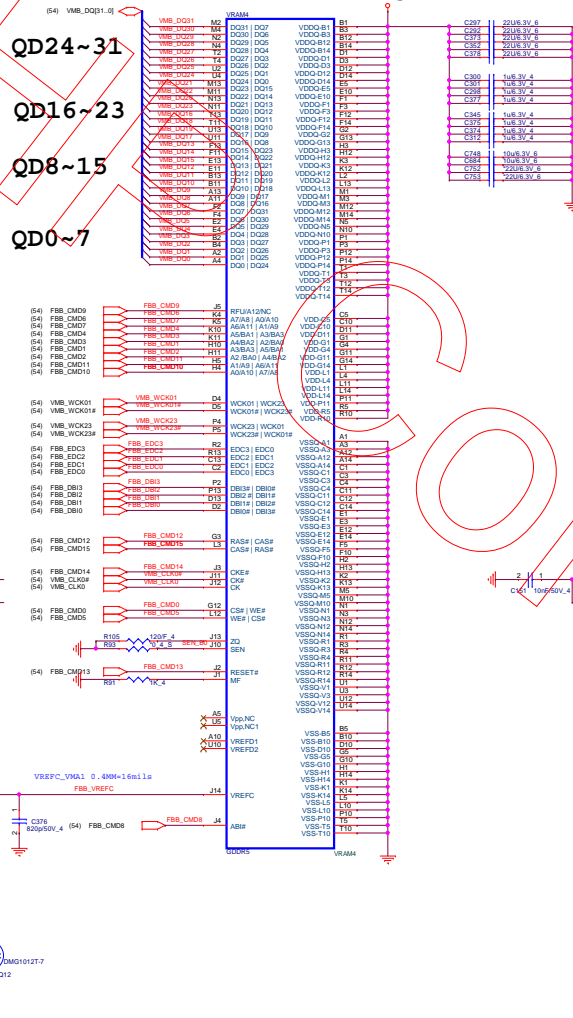


## CHANNEL B: 1024MB GDDR5x32

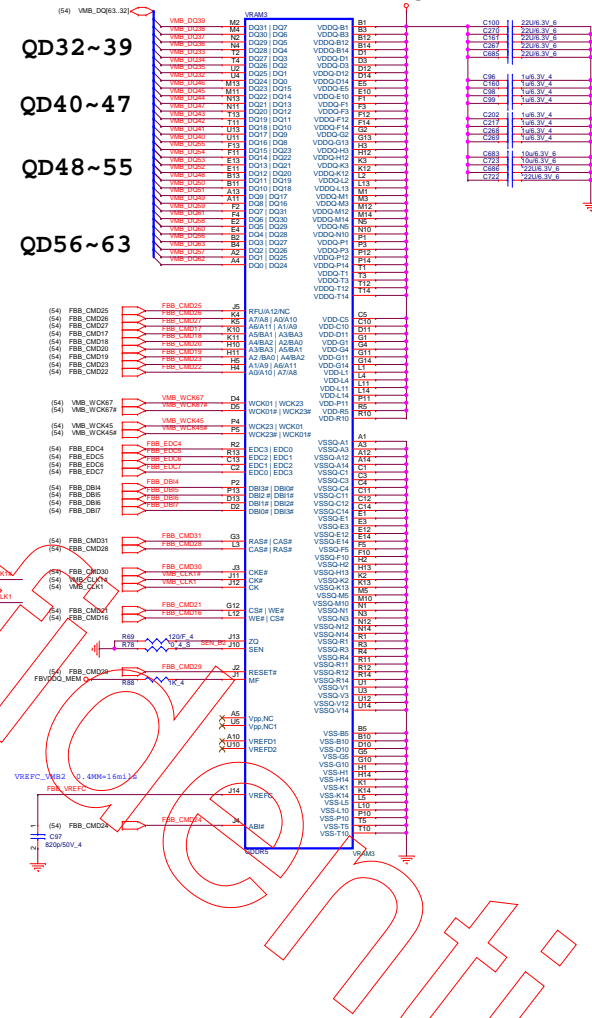
(47.51,54,56,57,58) FBVDDQ\_MEM

Channel B  
<0~31>

MF=0 Non-mirrored

Channel B  
<32~63>


MF=1 mirrored

PROJECT : G38A  
Quanta Computer Inc.

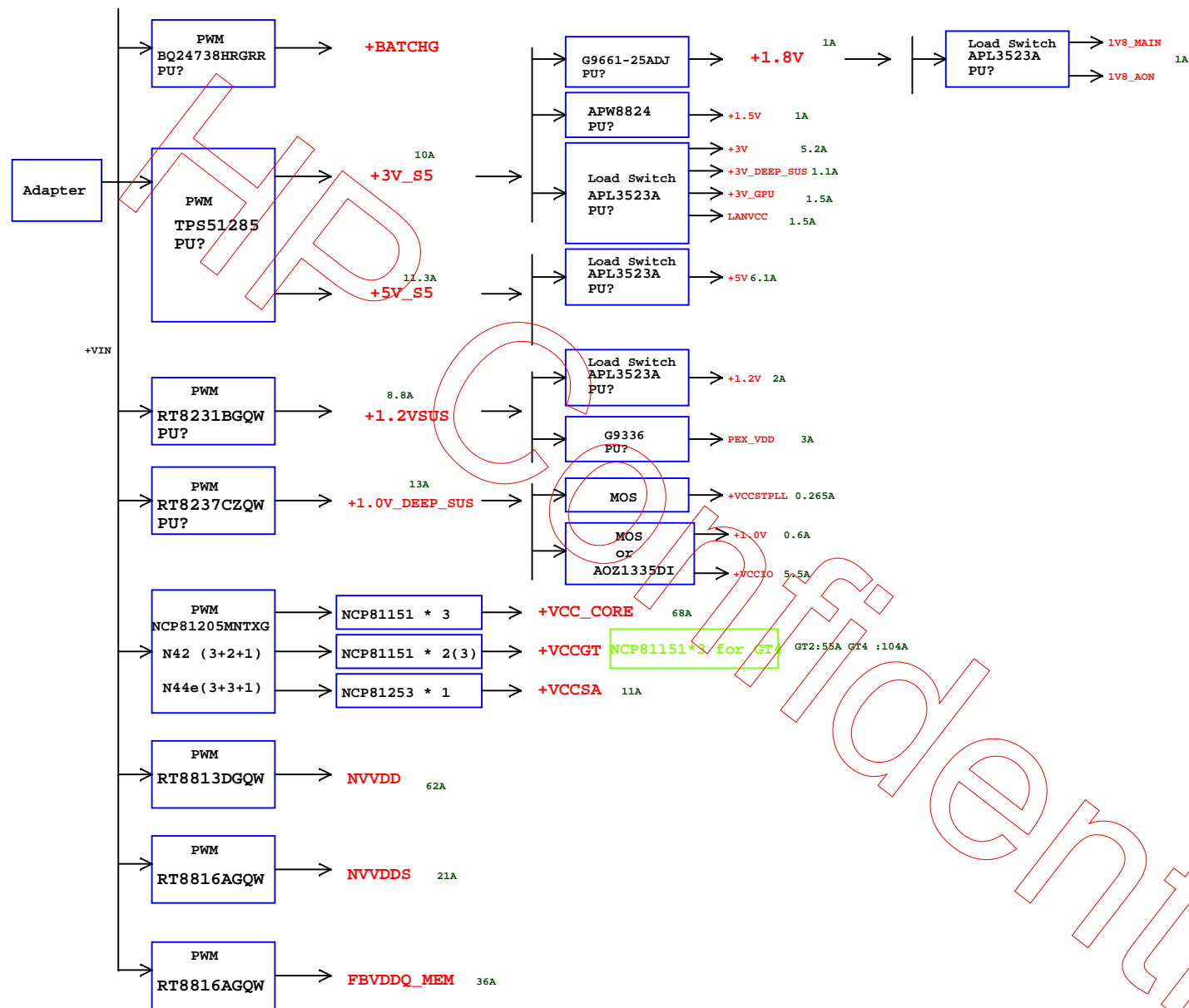
Doc	Document Number	Rev
NB5	N17E-QX-7(GDDR5)	1A
Date	Wednesday, October 18, 2017 (Sheet 59 of 66)	

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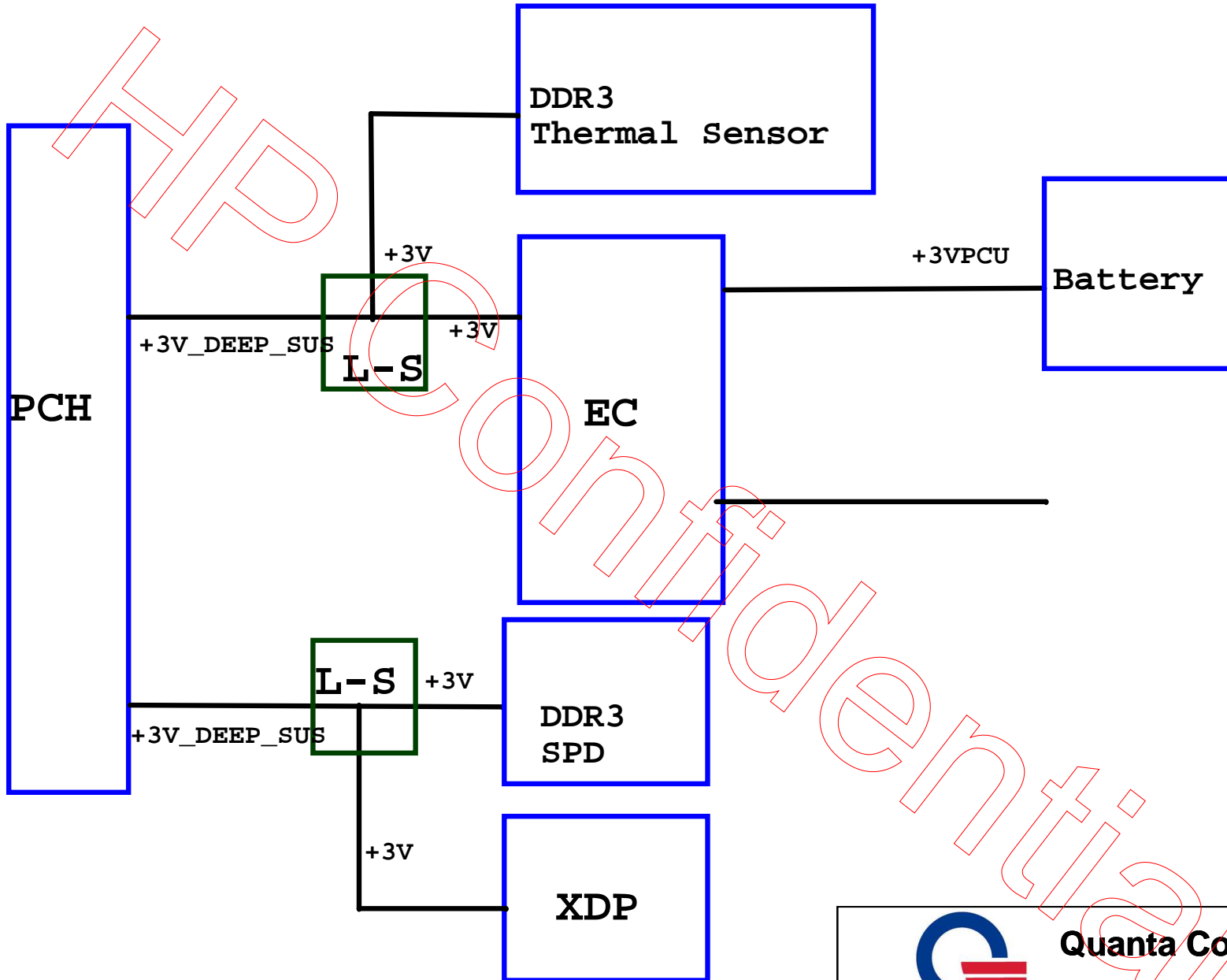
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		<b>Quanta Computer Inc.</b>	
<b>PROJECT :</b>			
Size Custom	Document Number	<b>blank</b>	Rev 3B
Date:	Monday, October 17, 2016		
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# Power Delivery Map



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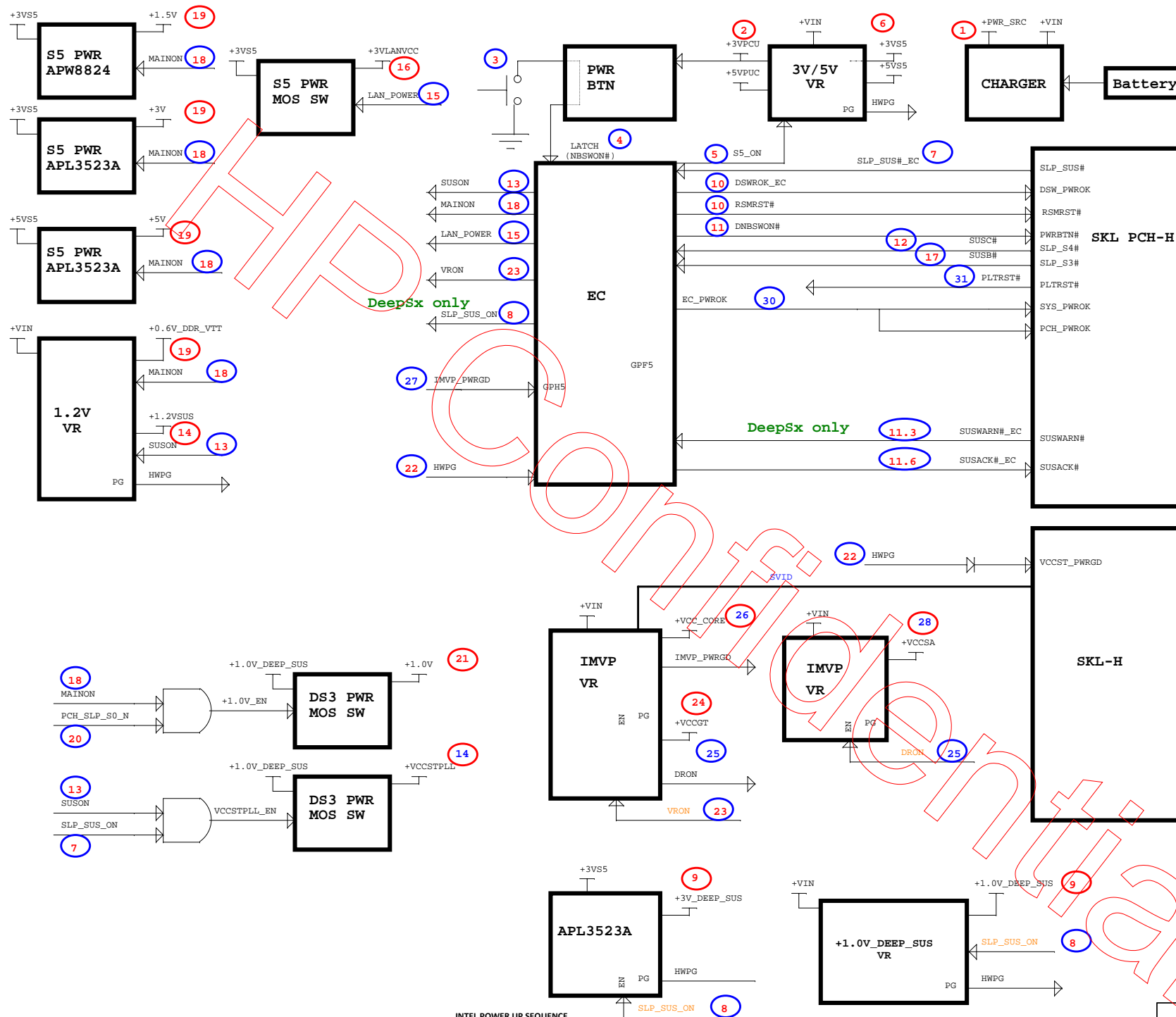
**Quanta Computer Inc.**

**PROJECT :**

Size A	Document Number <b>SMBus Map</b>	Rev 3B
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INTEL POWER UP SEQUENCE

2016

SDV

SIV

EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
EC-A-01	19	8/10	R760	DP_Power add 0 ohm
EC-A-02	19	8/10	Q70,R761,R762	DP_HPDP change to dual mos type
EC-A-03	20	8/10	R763	HDMI_Power add 0 ohm
EC-A-04	12	8/10	Add U52,del U53	BIOS change socket to rom for B test
EC-A-05	26	8/10	C835	change 0402 correct PN
EC-A-06	26	8/10	C509,Y2	change cap,crystal for vendor recommend
EC-A-07	53	8/10	U39	change PN for 2nd source team recommend
EC-A-08	18	8/10	CN6	change to Vertical type &FP and upsidedown pin order
EC-A-09	27	8/10	CN1	change to type-C FP
EC-A-10	9	8/10	Q71,Q72,R766,C934	change GC6EN circuit
EC-A-11	56	8/10	U55,U56,R767,R768,R769	GPU power down sequence
EC-A-12	56	8/11		change from OVERT# to DGPU_OVT#
EC-A-13	55	8/17		Reserve GPU external bios for debug use
EC-A-14	30	8/19	R778,R779,R458,R448,R776,R777	cypress review CCG2 to Mux can't have cap
EC-A-15	10	8/19	R246	EC S5 leakage form AC PRESENT
EC-A-16	2,10	8/19	R780,R781,R782,R783	xHCI Debug Capability Compliance issue
EC-A-17	28	9/6	R161,R620	change Ilim to 93.1k ohm for 3A,asm R161 for type c hpd open drain
EC-B-01	13,19	10/17	R784,C785,C803	for DP to hdmi dongle cable issue
EC-B-02	20	10/17	C10,C621	change 0805 size to 0402 size
EC-B-03	56	10/17	R568	for remove R568 NV PWRGD path
EC-B-04	27	10/19	C816,C936	for FAE suggest
EC-B-05	10	10/26	R246	For ME check fail issue

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Custom	EC-list-1		
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